ISSN :2277-2685
IJESR/APRIL. 2023/ Vol-13/Issue-2/1-8
**Mr.T.Ramesh , *et. al.* /International Journal of Engineering & Science**

# Design of Folded Cascode OTA in Different Regions of Operation Through $g_m/I_D$ Methodology

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***Abstract* —** In this study, we provide a systematic approach to the design of folded cascode operational transconductance amplifiers. In order to maximize the efficiency of the MOS transistors, the design is carried out in three distinct zones of operation (weak inversion, strong inversion, and moderate inversion) according to the gm/ID technique.
The developed folded cascode OTA operates in strong inversion mode with a unity-gain frequency of 430MHz and a DC gain of 77.5dB using a 0.35m CMOS technology. It offers a 92dB DC gain and a gain bandwidth product of around 69MHz when operating in a mild inversion mode. DC gain of 75.5 dB and unity-gain frequency are also characteristics of the OTA circuit.
In order to construct a Sigma Delta ADC for broad band radio applications, we set out to create a folded cascode OTA circuit.
This paper will proceed as described below. In Part II, we dissect the OTA structure of a folded cascode. The OTA circuit architecture for the three operating ranges is shown in Section III. Section IV provides a scope for the design. After comparing our research to other studies, we provide some final thoughts. weak inversion area restricts frequency to 19.14 MHZ.

## II. COMPACT OTA STRUCTURE

*A.* Folded Cascode OTA, CMOS IC design, and g / I

### *B. NMOS Input Transistor*

**INTRODUCTION**

M. D The gain of the operational amplifier is produced by its input stage. Since the NMOS device is more mobile, the input differential pair of a PMOS device experiences less noise. The evolution of the microelectronics sector has been marked by ever-increasing integration and complexity. Linear miniaturization of integrated circuit design characteristics is the target. Value of The design's intricacy is one of the main obstacles stopping this progression in its tracks. Building a reliable analogue IC requires the skill of an experienced designer. Although numerous tools have emerged over the years to help automate the topology synthesis [1]-[4], it is ultimately up to the designer to decide which circuit architecture is most suited to satisfy the needs. In [5], we see the establishment of a successful heuristic approach to optimization. References [6]–[7] cover the literature on nominal circuit design, [8–10] cover size concerns, and [11–13] cover worst-case optimization. There are a number of optimization programs available, including the equation-based GPCAD [14, 15], the symbolic-based AMG [16, 17], and the simulation-based ASTRX/OBLX [17, 18]. Multiple recent articles ([13], [19]-[24]) have addressed the size problem from a variety of angles. While we have made strides toward lower supply voltages and higher frequencies, it is still difficult to develop high-performance base band analog circuits. Software-based radio receivers that anticipate an after-antenna RF signal conversion are now popular. Therefore, a substantially greater sampling frequency and resolution are required in the design of the analog-to-digital converter. In this case, the OTA is a an essential component of this kind of circuit, whether or not the switched capacitors method is employed to create the ADC. an NMOS pair with higher transconductance than the carrier. Because of this need for maximum gain, an NMOS transistor was used.

### B. Analysis of the Structure

The operational amplifier is the most time-consuming part of an analog circuit. The designer has a variety of OTA configurations to choose from, most of which are geared on raising the bar for performance expectations in design [25]. For its high gain and wide bandwidth, a "folded cascode" op-amp is our top pick. The folded cascode OTA is shown in Fig.1 (the term "folded cascode" refers to the modification of a diff-pair's Mosfets from p-channels to n-channels, thus the name).

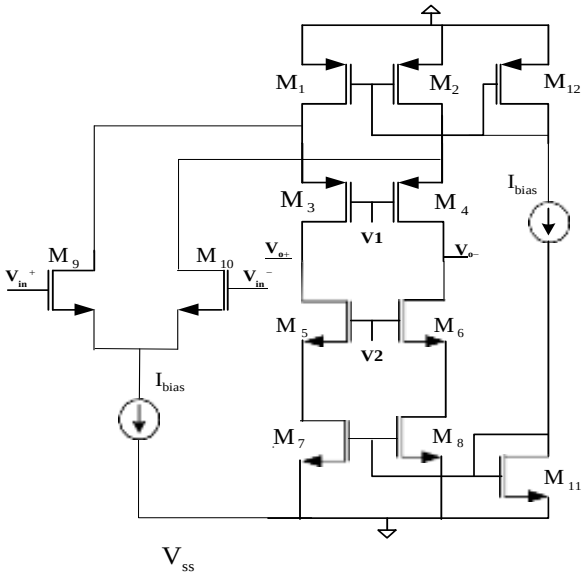


Fig. 1 Folded cascode OTA topology

A differential stage, made up of NMOS transistors M9 and M10, is essential to the functioning of the folded cascode OTA. Transistors M1, M2, M7, and M8 get their DC bias voltages from mosfets M11 and M12. Gain bandwidth and open-loop voltage gain are defined as follows: (1)

A = g m9.g m6.g m4 V I 2 g 2 + g 2 D m 4 N m 6 P (1)

GBW = g m9 ID

ID C L (2)

Where gm4, gm6, and gm9 are the transconductances of the M4, M6, and M9 transistors, respectively. Mosfets M4, M6, and M9 all have a bias current, denoted by ID. The parameters N and P refer to channel length modulation for NMOS and PMOS devices, respectively; CL denotes the capacitance at the output node. With M4 and M6 transistors' complementary nature in mind:

gm4 = gm 6 (3)

This leads to the following gain expression: A = g m 9. g m 6 V I 2 2 + 2 D N P (4)

Twelfth, a folded cascade OTA layout

Different aspects of the op-amp's functionality—such as its open-loop voltage gain, unity-gain bandwidth, slew rate, noise, and so on—are what set it apart. These performance metrics, such as transistor size, bias currents, and other component quantities, are hardcoded into the design [26].

Finding the optimal values for design parameters that nevertheless adhere to requirements and other guidelines is the focus of this effort. In this work, we present the layout of a foldable cascode OTA amplifier that can function in one of three frequency bands. The gm/ID approach proposed by Flandre and Silveira [27] is used in this design's synthesis technique.

A Measurement Formulation

To better understand the top-down synthesis process for CMOS OTA structures, a design flow has been created (Fig. 2). In reality, this last step begins with setting the criteria to optimize, such gain and unity gain frequency, so that MOS device sizes and bias current may be calculated.

• gm9 may be calculated directly from the transition frequency and capacitive load using equation (2), whereas gm9/ID can be calculated using equation (4) utilizing the supplied DC open-loop gain and the selected technology. The bias current, ID, may be calculated using either gm9 or gm9/ID, and gm9/ID also returns I', where I'= ID/(W /L).

ID/I' provides the final answer for W/L To use the aforementioned technique and calculate the design parameters (Fig. 3), we take advantage of the fact that the CMOS technology at hand (0.35m of AMS) exhibits a universal gm/ID as a function of ID/(W/L). This feature is gained by modeling and is formally specified in the

ISSN :2277-2685
IJESR/APRIL. 2023/ Vol-13/Issue-2/1-8
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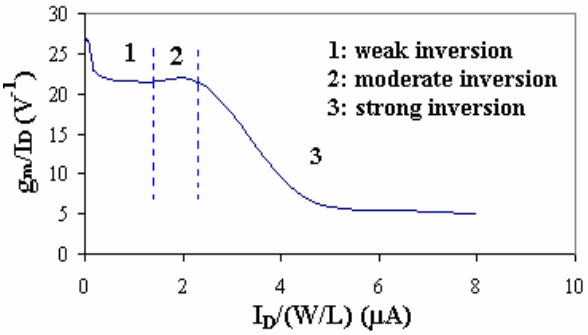



C: Weak Inversion

All of the transistor's capabilities, whether weak,

Fig.3 $g_m/I_D$ as a function of $I_D/(W/L)$

Region moderate, or strong inversion, linear, or saturated mode, quasi-static, or high-frequency operation, may be used to their fullest extent [30].

In analogue circuits, the transistors are often biased in the saturation state. However, either strong or weak inversion may be used to run them. Biased in weak inversion, transistors give more gain with less current and have a greater transconductance. The thermal noise produced by these transistors is minimal. We want to provide a method to analyze folded cascode OTA performance across all three modes of operation.

D. Weak Inversion Design

Weak inversion exhibits larger gm/ID values with lower current, as illustrated in Fig. 4. Consequently, a greater gain is preferable for this working mode.

Our requirements for the circuit shown in Fig.1 are listed in Table I.

TABLE I
SPECIFICATIONS

| Specifications | Values |
|---|---|
| $A_v$ (dB) | 105 |
| GBW (MHz) | 21.5 |
| $C_L$ (fF) | 10 |
| $V_{dd}/V_{ss}$ (V) | ±1 |
| Channel length (µm) | 1 |

Applying the previously elucidated design technique, we get the calculated and summarized parameters in table II.TABLE II
DESIGN PARAMETERS IN WEAK INVERSION

TABLE III
SPECIFICATIONS

| Specifications | Values |
|---|---|
| $A_v$ (dB) | 100 |
| GBW (MHz) | 70 |
| $C_L$ (pF) | 0.1 |
| $V_{dd}/V_{ss}$ (V) | ±2 |
| Channel length (µm) | 1 |

| Parameters | Values |
|---|---|
| $I_D$ (nA) | 50 |
| $W_{9,10}$ (µm) | 3.5 |
| $W_{3,4}$ (µm) | 2.7 |
| $W_{5,6,7,8}$ (µm) | 1 |
| $W_{1,2,12}$ (µm) | 5.4 |
| $W_{11}$ (µm) | 2 |
| $V_1 = V_2$ (mV) | -428 |

Similarly, the design technique mentioned in Section A is used to ensure that the tiny signals model remains unchanged over all sections of the transistor's operational spectrum. The discovered design parameters

The designed folded cascode OTA is biased at ±1V powersupply voltage using CMOS technology of 0.35 µm of AMS

TABLE IV

with the BSIM3V3 MOSFET model. The circuit denotes an offset voltage of 0.4mV, a Slew Rate of 3.3V/µs, a wide input common-mode range of [-0.99V, 0.98V], a wide output common-mode range between -0.96V and 0.95V. It consumes 0.6µW.

Moreover, our device is able to achieve a degrading gain of 75.5dB, a bandwidth of 19.14MHz with phase margin of 67degrees (Fig.4), a good common mode rejection ratio of 126.8dB and a low transconductance of 1.8µS kept constant for a wide range of frequency (Fig.5).

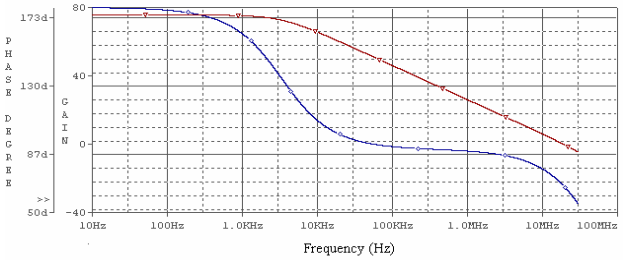



Fig.4 Gain and phase curve

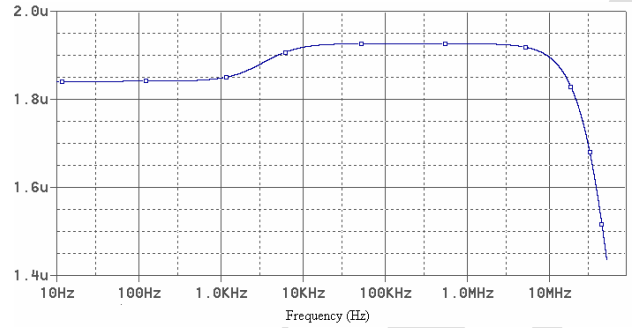



Fig.5 OTA's transconductance in weak inversion region

*Moderate Inversion C. Design*
*Consequently, the gain bandwidth product isn't increased and essential enough to suit wide band applications since we get excellent performances with extremely low consumption in weak inversion.*
*We will analyze the OTA's design in the mild inversion zone to see if we can increase this parameter while maintaining the same level of energy efficiency. In order to further restrict the bandwidth product of the OTA gain, we suggest the requirements shown in table III.*

DESIGN PARAMETERS IN MODERATE INVERSION

| Parameters | Values | |
|---|---|---|
| $I_D$ (µA) | 2 | |
| $W_{9,10}$ (µm) | 9 | |
| $W_{3,4}$ (µm) | | 2.7 |
| $W_{5,6,7,8}$ (µm) | 1 | |
| $W_{1,2,12}$ (µm) | | 5.4 |
| $W_{11}$ (µm) | 2 | |
| $V_1 = V_2$ (mV) | -256 | |

Fig.6 shows that the OTA circuit can achieve a DC gain of 92dB, a unity-gain frequency of 69MHz, and a phase margin of 74.5degrees. Figure 7 depicts its transconductance value of around 65 S. It loses 48 mW of power.
Gain and GBW characteristics are intriguing in this behavior mode, as are the broad input and output swings that are preserved.

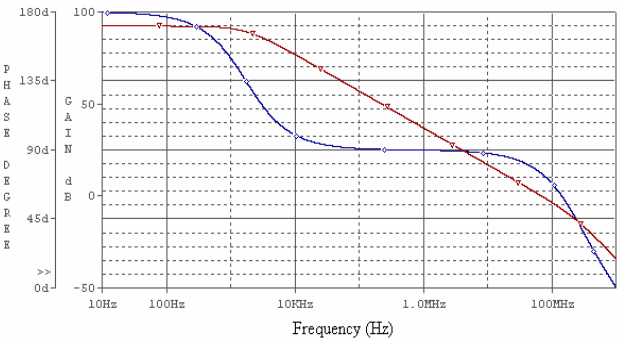



Fig.6 Gain and phase curve

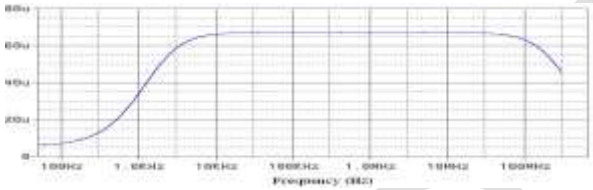
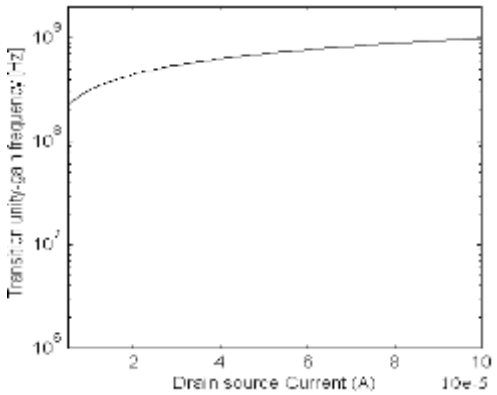


Fig.7 OTA's transconductance in moderate inversion region

*C. Layout for Extreme Inversion*

*We estimate that bandwidths fulfilling the needs of wide band applications may be attained even in weak inversion and for relatively large bias current.*

*In this current range, we see that the gm/ID ratio decreases with increasing current. Then, we put in a*




specifications given by table V.

TABLE V
SPECIFICATIONS

| Caractéristiques | Valeurs |
|---|---|
| $A_v$ (dB) | 80 |
| GBW (MHz) | 450 |
| $C_L$ (pF) | 0.1 |
| $V_{dd}/V_{ss}$ (V) | ±2 |
| Channel length (µm) | 1 |

The design process yields the Mosfets' sizes (table VI). The results of strong inversion, we conclude, are more relevant than those of weak and moderate inversion, and this is because strong inversion makes advantage of high current to reach other places.

Fig.9 Unity gain frequency as a function of drain source

TABLE VI
DESIGN PARAMETERS IN STRONG INVERSION

| Parameters | Values |
|---|---|
| $I_D$ (µA) | 27.5 |
| $W_{9,10}$ (µm) | 14 |
| $W_{3,4}$ (µm) | 5.4 |

| | |
|---|---|
| $W_{5,6,7,8}$ (µm) | 2 |
| $W_{1,2,12}$ (µm) | 10.8 |
| $W_{11}$ (µm) | 4 |
| $V_1 = V_2$ (mV) | -318 |

Featuring a huge unity-gain frequency of 430MHz and a phase margin of 58.2degrees, the folded cascode OTA has a gain of 77.5dB. Approximately 396 S may be transducted via it (Fig. 8).

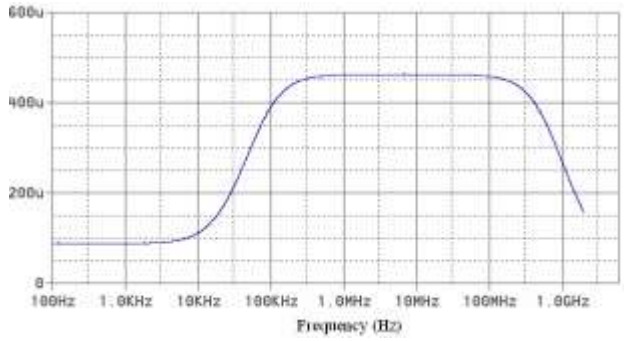



Fig.8 OTA's transconductance in strong inversion region

The folded cascode OTA design phase included the presentation of a number of features (table.VII). This architecture is functional in a wide range of frequencies. The transistor operating mode is determined by the requirements of the application.

VISUALIZATION PANEL XII

We use the MATLAB tool to show a design window in several areas of operation, each of which produces a unique pair of (Ft, ID) values that may be used to check certain design parameters, such as the unity gain frequency and the drain source current.

In strong inversion, a drain current of 27.5A results in a unity-gain frequency of 460MHz, as shown in Figs.9 and 10. For a constant 2A current, the GBW value is close to 90MHz when the inversion is modest.

In the mild inversion area, we see that the unity gain frequency rises, thus we must account for the modification of the signals model in this region strong inversion current

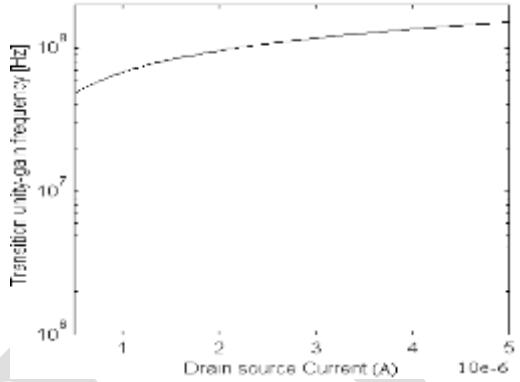



Fig.10 Unity gain frequency as a function of drain source current inmoderate inversion region

III. Results Comparisons (XII)

IV. We will compare our research to previous studies after we explain the various OTA design factors. This paper compares the folded cascode OTA's performance to that of two recently designed OTA circuits. Class-AB OTAs are the initial kind [29].Second, in [30], a telescoping OTA design was introduced. Table VIII provides this contrast. It can be easily observed that a low power, low voltage topology with a high static gain may be attained by using a folded cascode OTA design.

XVI. CONCLUSIONS

As a result, the synthesis of high-performance analog integrated circuits is a challenging endeavor that requires expert knowledge of a wide range of topics. Therefore, the skill set of the analog designer is still highly sought for. To achieve high gain and wide bandwidth, this paper discusses the strategy design of a folded cascode OTA operating in weak inversion, strong inversion, and moderate inversion.

We predict that the gm/ID approach is widely used for sizing in a variety of operational modes, allowing for the highest possible performance with any given technology.

Using these findings on folded cascode OTA for low consumption and broad band applications in wide band A/D converters is a potential direction for further research.

TABLE VII
FOLDED CASCODE OTA SPECIFICATIONS

| Specifications | Weak inversion | Moderate inversion | Strong inversion |
|---|---|---|---|
| DC Gain (dB) | 75.57 | 92 | 77.53 |
| GBW (MHz) | 19.14 | 69 | 430 |
| Transconductance (µS) | 1.8 | 65 | 396 |
| Phase margin (degrees) | 67 | 74.5 | 58 |
| Offset voltage (µV) | 430.4 | 246 | 337 |
| Output swing (V) | [-0.96 ; 0.95] | [-1.94 ; 1.84] | [-1.84 ; 1.72] |
| Input swing (V) | [-0.99 ; 0.98] | [-1.95 ; 1.87] | [-1.95 ; 1.87] |
| Slew Rate (V/µs) | 3.3 | 16.5 | 196 |
| CMRR (dB) | 126.8 | 133 | 114 |
| PSRR p, n (dB) | 18 | 45.7 | 46.5 |
| Supply voltage (V) | ±1 | ±2 | ±2 |
| Bias current (µA) | 0.1 4 | | 55 |
| Power consumption (µW) | 0.6 | 48 | 660 |

TABLE VIII
PERFORMANCES COMPARISON

| Performance/Design | Yao & Steyaert [29] | Craig Brendan Keogh [30] | This work |
|---|---|---|---|
| OTA Architecture | Class-AB | Telescopic | Folded cascode |
| Technology (µm) | 0.09 | 0.18 | 0.35 |
| DC Gain (dB) | 50 | 79 | 75.57 |
| GBW (MHz) | 57 | 8.5 | 19.14 |
| Phase margin (degrees) | 57 | 78 | 67 |
| Supply voltage (V) | 1 | 0.925 1 | |
| Power consumption (µW) | 80 | 4.6 | 0.6 |

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In his article "Low-Power Multi-Bit -Modulator Design for portable Audio Application," Craig Brendan Keogh presented research from Stockholm in March 2005.