

Bidirectional High-Efficiency Converter with Common-Mode Decoupling for AC and DC Grid Interconnection

Mr.J.Stanly Selva Kumar stanly@stellamaryscoe.edu.in

Dr.A.R.Gayathri GAYATHRI@stellamaryscoe.edu.in

Dr.K.Ezhil Vignesh ezhilvignesh@stellamaryscoe.edu.in

Mrs.J.Jasmine jasmine@stellamaryscoe.edu.in

Mr.C.Suyambulinga Rajan suyambulingarajan@stellamaryscoe.edu.in

**Department of Electrical and Electronics Engineering
Stella Mary's College Of Engineering, Tamilnadu, India**

Abstract— This paper presents an interface ac-dc converter to connect the 380 V bipolar dc microgrid with the 240 V split-phase single-phase ac utility. The design targets are high efficiency, leakage current attenuation and symmetric bipolar dc bus generation. A transformerless two-stage topology is proposed to decouple the common-mode (CM) voltage between the connected ac and dc systems. The two-stage structure also reduces the required capacitance in single-phase power conversion by allowing a large voltage ripple on the intermediate dc-link. Adaptive dc-link voltage control and interleaving of state-of-the-art silicon carbide (SiC) MOSFETs are adopted to achieve high efficiency. Interleaving angles are optimized to minimize the total volume of both differential-mode and CM magnetics. An active CM control method is incorporated to regulate the dc and low-frequency CM voltages on the dc buses with respect to the ground. The resultant dc bus voltages are rendered symmetric to the ground, and the leakage current is suppressed. The generated ± 190 V dc bus is suitable for bipolar 380 V dc power distribution systems. Pluggable phase-leg modules with embedded driving and protection circuit are designed and tested, based on which a 10 kW all-SiC converter prototype is built achieving an efficiency $> 97\%$.

Index Terms— Ac-dc converter; common-mode; leakage current; dc microgrids; efficiency; interleaving; silicon carbide (SiC).

1. INTRODUCTION

To integrate renewable sources and energy storage, dc power distribution has arisen as an attractive solution due to its simpler structure and higher efficiency than ac distribution [1]–[7].

Since most residential and consumer electronic appliances use dc voltage intrinsically, dc power distribution provides an opportunity to eliminate the back and forth dc-ac and ac-dc power conversions within a dc grid. The dc grid can be connected to the ac utility through an interface converter at the point of common coupling (PCC) and exchanges only the net energy [8]–[12]. Fig. 1 shows the schematic of a possible future residential dc power distribution system. Renewable energy sources, energy storage, and different kinds of loads

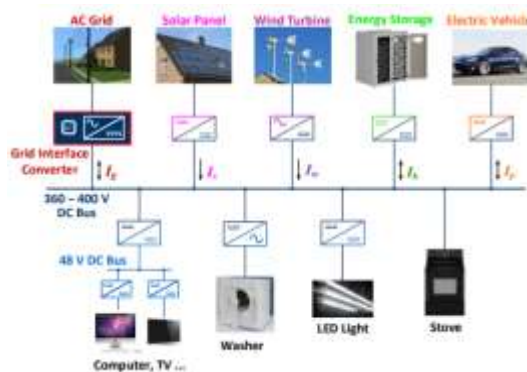


Fig. 1. DC power distribution in a future home.

are connected to a common dc bus through power converters. These converters not only match the outputs of different sources to the dc bus voltage, but also function as “dc fuses” to limit the fault current during bus short circuit, especially for sources like batteries. The dc system is connected to the ac utility through a bidirectional ac-dc grid-interface converter. The target power rating of this ac-dc converter is 10 kVA to cover the consumption of a single U.S. family.

In the system-level energy management, the interface converter functions as the brain of the dc grid; it exchanges information with the ac grid and is responsible for the optimization of energy utilization in the dc system. Thus the converter has been named the Energy Control Center (ECC) [10]–[12]. It is preferable to have the ECC regulate the dc bus voltage in a droop manner, i.e., reducing its output voltage when the output current increases, so different energy sources in a dc microgrid can share the total system load in proportion to their droop resistances. Besides, the dc bus voltage varies depending on the system load. By sensing the bus voltage, each source and load makes its own power management decision, giving an opportunity to optimize the system energy utilization without communication links [13], [14].

While isolation is usually required in high-power highvoltage applications, transformerless converters are appealing for low-power grid-tied dc systems in residential and some commercial facilities, such as small-scale photovoltaic (PV) generation [15], [16]. The benefits of using transformerless converters include size and cost reduction, and efficiency improvement by eliminating the line-frequency and highfrequency transformers.

However, using a non-isolated interface converter introduces a low impedance common-mode (CM) path between grounded ac and dc systems. In such architecture, the ac and dc CM quantities are coupled through the power converter and the ground. Depending on the impedance within this CM path, the resultant CM current may be significant, jeopardizing human safety and accelerating component aging. To attenuate the CM voltage, different active and passive methods have been discussed in literature, particularly for PV inverters because of the large parasitic capacitance between PV panels and ground. Topologies such as the highly efficient and reliable inverter concept (HERIC), H6 and neutral-point clamped (NPC) topologies have been evaluated to reduce the CM noise generation [17]–[19]. By adding extra switches to the circuit, the ac and dc sides of the power converter are separated during the free-wheeling state; the CM issue is relieved at the expense of higher circuit complexity and lower efficiency. Different modulation schemes have been proposed to reduce the CM voltage variation in [20]–[23], and a closedloop gate voltage control is used to limit the switching speed and EMI in [24], [25]. Another way to attenuate CM current is to change its transmission path. Traditional filters increase the CM path impedance so the measured output noise is reduced. In contrast, [11], [26], [27] propose using floating filters in gridtied converter and motor drive applications. The floating filter creates a low-impedance CM path to trap the CM noise within the converter instead of emitting to the output. Thus the measured noise at the output is reduced. While the high-frequency CM noise can be filtered by passive components, the dc and low-frequency CM voltage needs effective control to generate symmetric dc bus voltages for bipolar dc microgrids and mitigate the leakage current. An active CM control method using duty cycle injection is proposed in [28], but it requires knowledge of the system CM transfer function, and can only generate symmetric dc buses for certain ac interfaces. A high-density transformerless two-stage bidirectional acdc converter (ECC Gen 1) is developed in [10], [11]. Its key feature is to allow a large voltage ripple on the intermediate dc link, which greatly reduces the inherently large dc bus

capacitance in single-phase ac-dc power converters. To handle the higher dc bus ripple, 1.2 kV IGBTs are used at the expense of higher switching losses. As a result, the measured efficiency is lower than 90 % with a 20 kHz switching frequency. Modified versions of ECC have been discussed in [29], [30] to improve its CM performance with and without floating filter. However, the passive filter design and efficiency improvement have not been fully addressed. In this study, the goal is to develop a high-efficiency and high-density transformerless ac-dc interface converter (ECC Gen 2) to connect 380 V dc systems with split-phase 240 V residential ac grids. Compared to the aforementioned techniques, the proposed two-stage topology along with its CM controller simultaneously achieves the reduction of double-line-frequency capacitance in single-phase ac-dc power conversion and the CM voltage decoupling between the ac and dc grids. An adaptive dc-link voltage control and

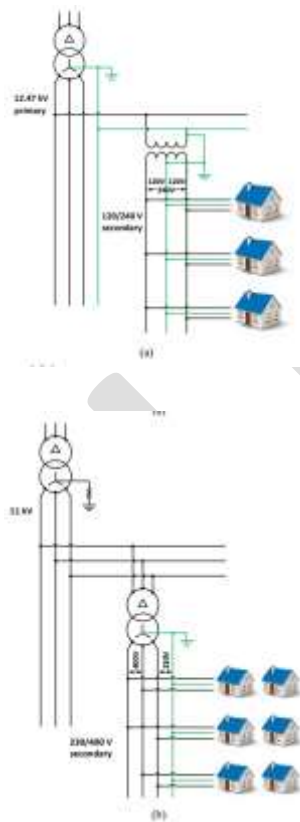


Fig. 2. AC power distribution layouts. (a) North America. (b) Europe

interleaved SiC MOSFETs are adopted to achieve a high efficiency. Interleaving angles are optimized to reduce the size of both DM and CM magnetics. An active CM duty cycle injection method is incorporated to control the dc and lowfrequency CM voltages on the dc side buses. A pluggable phase-leg module is designed, based on which a 10 kW converter prototype is built achieving an efficiency $> 97\%$.

2. CM VOLTAGE AND LEAKAGE CURRENT FOR GROUNDED SYSTEMS CONNECTED BY NON-ISOLATED POWER CONVERTERS

The grounding scheme is critical when ac and dc grids are connected. Fig. 2 presents the typical structures of the ac power distribution systems in North America and Europe. In the U.S., medium-voltage (MV) distribution uses a three- phase four-wire system. The low-voltage distribution is fed from one phase of the MV distribution. The residential interface is a split-phase system. The phase-to-neutral voltage is 120 V rms for lighting and pluggable loads; the line-to-line voltage is 240 V rms for heavy loads such as heaters, electric ranges, and air conditioner units. The neutral line is grounded at the distribution transformer. The green lines highlight the ground connection. In Europe, electricity is normally distributed for domestic use by a three-phase four-wire system. Most of the countries adopt a line-to-line voltage of 400 V and a line-to-neutral voltage of 230 V 50 Hz. On the dc side, the lack of standards have led to different voltage levels and grounding schemes [31]–[34]. One broadly used configuration is 380 V for home appliances and 48 V for telecommunication equipment. The dc system can be unipolar or bipolar depending on the grounding method. In the unipolar scheme, one of the active lines is grounded. In the bipolar case, a middle line between the positive and negative buses is grounded. In the latter case, the voltage on the positive and negative line to the ground is only half of the total bus voltage, which makes it safer for residents; thus the bipolar scheme is adopted in this work. According to IEC 60364-1, grounding schemes can be classified as TN, TT and IT, in which the first letter refers to the source grounding (T – solidly, I – indirect) and the second letter refers to the load grounding (T – individual grounding wire, N – grounded through neutral wire). In this work, the source side, which is the dc output of the interface ac-dc converter, is grounded so the system can be TN or TT. Fig. 3 shows one TN grounding configuration for bipolar dc distribution, where PE refers to the protective earth wire. The neutral

line N and PE are combined at the source side, forming the PEN line. Both the ac and dc systems are grounded in the aforementioned schemes. If the interface converter is not isolated, a leakage current, i.e., CM current, flows through the interface converter and the common ground, as shown in Fig. 4, introducing additional losses and accelerating the ageing of components. As highlighted in [5], the CM voltage and leakage current are related to each other by the grounding impedance. For a very high ground impedance, there will be no leakage current, but the CM voltage will be at its maximum. In contrast, if the system is solidly grounded, there will be no CM voltage, but the leakage current will be the highest.

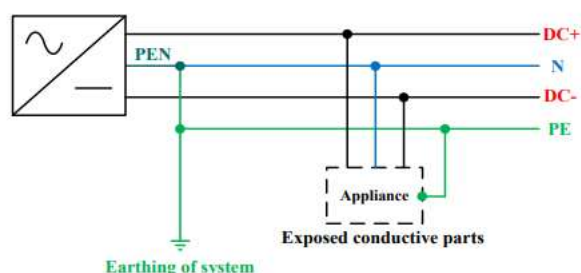


Fig. 3. DC power distribution system using TN grounding scheme.

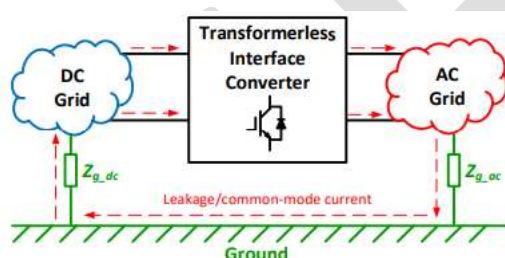


Fig. 4. Common-mode current circulating between interconnected ac and dc systems.

3. TWO-STAGE CONVERTER TO DECOUPLE THE CM VOLTAGE

To decouple the CM voltages between the connected ac and dc systems, a two-stage symmetric converter topology is shown in Fig. 5. The converter includes a full-bridge ac-dc stage and a full-bridge dc-dc stage. The ac-dc stage regulates the ac current and the dc-link voltage. The steady-state dc-link voltage has a large voltage ripple to reduce the capacitors for double-line frequency power ripple. As discussed in [10], the capacitance can be reduced by more than 10 times. This enables a size reduction and prolongs the converter lifetime by replacing electrolytic capacitors

with film ones. The fullbridge dc-dc stage steps down the dc-link voltage and generates a symmetric dc bus. Both of the stages are power bidirectional. It is worth noting that even though the two-level H-bridge is used as an example, the phase-leg can also adopt multi-level or interleaved structures. On the ac side, L_{D_ac} , C_{D_ac} and L_{g_ac} serve as the ac-side differential-mode (DM) filter. On the dc side, L_{D_dc} , C_{D_dc} and L_{g_dc} serve as the dc-side DM filter. The blue components, L_{C_ac} , C_{C_ac} , L_{C_dc} and C_{C_dc} , constitute the CM filter on the ac and dc sides, respectively. As shown by the green line, the ground of the ac and dc sides are physically connected at the

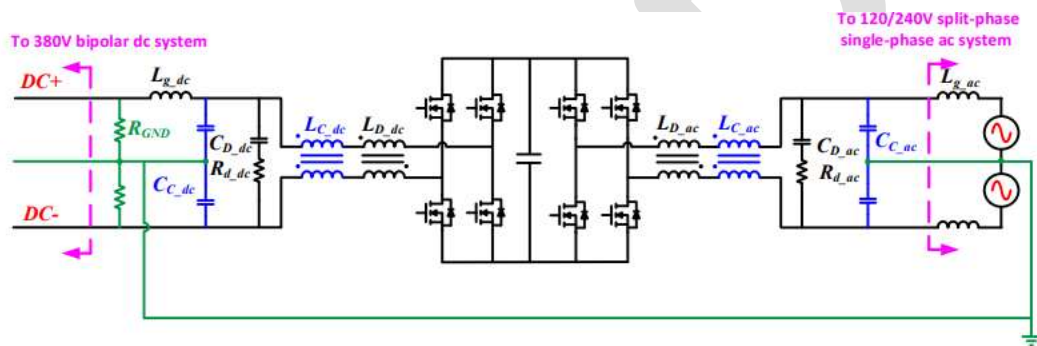


Fig. 5. Two-stage bidirectional single-phase ac-dc converter with common-mode decoupling.

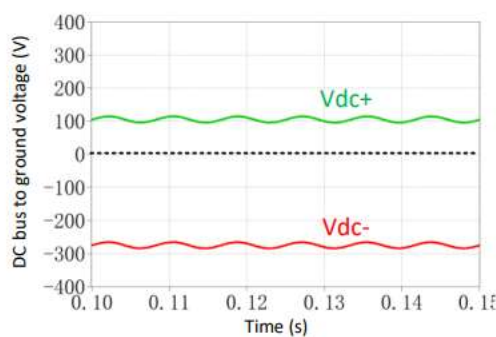


Fig. 6. Asymmetric dc bus to ground voltages using the half-bridge dc-dc in [10]. (Note: The DM positive to negative bus voltage is 380 V without ripple)

Compared with [10]–[12], which use a half-bridge for the dc-dc stage, using a full-bridge enables the decoupling of the ac- and dc-side CM voltages. If only a half-bridge is used for the dc-dc

stage, the dc-side bus-to-ground voltage depends on the ac-side grounding. If the mid-point of the ac is grounded, then the dc buses have positive and negative voltages to the ground with different magnitudes, as shown in Fig. 6. Even if we assume the positive and negative dc-link voltages are symmetric to the ground, the dc bus voltages will not be symmetric because only the positive bus is modulated. On the other hand, using a full-bridge dc-dc, both the positive and negative dc bus voltages are modulated and can be regulated at any value between the positive and negative dc-link voltages. Consequently, the converter has more flexibility in controlling the dc bus to ground voltages. Another important requirement for the interface converter is high efficiency. The interface converter functions as an energy router to balance the power between the ac and dc grids. The router itself should be very efficient, especially under light load, since that is where the converter operates most of the time. To achieve a high-efficiency power stage design, the converter efficiency has been evaluated using different two-level and three-level phase-leg structures and state-of-the-art Si and SiC power devices. The results are presented in [35]. In summary, the two-level full-bridge with two paralleled 25 mΩ SiC MOSFETs working at 40 kHz strikes a good balance between conduction and switching losses. Since interleaving has the benefit of reducing the size of passive components, two-phase interleaving is chosen as the final design to achieve high efficiency and power density. The complete power stage schematic is shown in Fig. 7. The

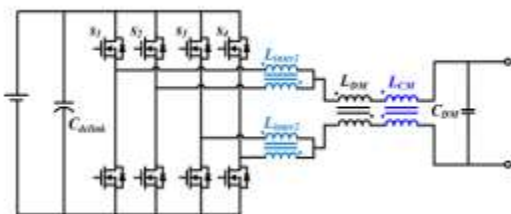


Fig. 8. Circuit to derive the design constraints for magnetic components.

device is the state-of-the-art, commercial 1.2 kV, 25 mΩ SiC MOSFET C2M0025120D from Wolfspeed.

4. VOLUME MINIMIZATION FOR MAGNETICS WITH OPTIMIZED INTERLEAVING ANGLES

To guarantee high power quality and satisfy applicable requirements, DM and CM filters need to be designed. Depending on the voltage and current stress, each component has different design constraints. In this section, the stress for each inductive component is analyzed, based on which magnetic components are designed. As presented, the two-stage converter uses a symmetric ac-dc and dc-dc structure. To explain the design principle, the design procedure is presented for the interleaved full-bridge converter shown in Fig. 8 without any constraint on the modulation or duty cycle. After deriving the fundamental equations, the operating condition for each component under either ac-dc or dc-dc operation can be substituted into these equations to generate a specific design. In the figure, Linter1 and Linter2 are the interphase inductors that reduce circulating current between the interleaved phase-legs, LDM is the DM inductor that limits the DM current ripple, LCM is the CM choke, Cdclink and CDM are the DM capacitors on each side.

The inductive components take up a lot of space in the whole system. The volt-seconds on these components are used to estimate their size with different interleaving angles; then the total filter size can be optimized. For the interphase inductor Linter1, Linter2 and CM choke LCM, the design procedures are similar. Neither of these inductors bears high dc bias current, so the design constraint mainly depends on the core saturation from the switching cycle volt-second. The technique of using volt-second to

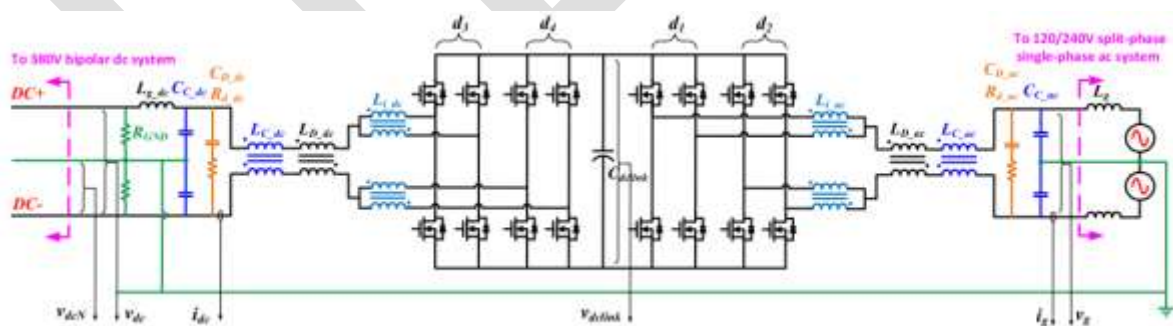


Fig. 7. Interleaved two-stage converter with filters and control sampling.

analyze CM inductor saturation has been discussed for motor drive in [36] as well. In some cases, the core loss can also be a limit. However, the switching frequency is below 100 kHz and a low-loss core material is selected in this design, so the main constraint is considered to be saturation.

By Faraday's law,

$$v = N \frac{d\phi}{dt} = NA_c \frac{dB}{dt}$$

where v is the voltage applied on the inductive component, N is the number of turns of the winding, A_c is the core crosssectional area, Φ is the flux through the winding, B is the flux density, and t is time. Multiplying (1) by dt and integrating both sides of the equation gives

$$\int v dt = \int NA_c dB$$

The left-hand side is the total applied volt-second to the inductor. To avoid core saturation, the core and winding need to satisfy

$$VS_{\max} < NA_c B_{\max}$$

where VS_{\max} is the applied maximum volt-second during every switching cycle, and B_{\max} is the allowed maximum flux density for the core material. The size of the inductor can accordingly be expressed as

$$NA_c > \frac{VS_{\max}}{B_{\max}}$$

or in the area product form

$$W_a A_c > \frac{I_{rms}}{J \cdot K_u} \cdot \frac{VS_{\max}}{B_{\max}}$$

where W_a is the window area of the core, I_{rms} is the rms value of the current conducted through the winding, J is the current density for the wire, and K_u is the filling factor of the core window area. For the DM inductor, usually the maximum current going through the inductor determines the maximum flux density and thus the volume, which means

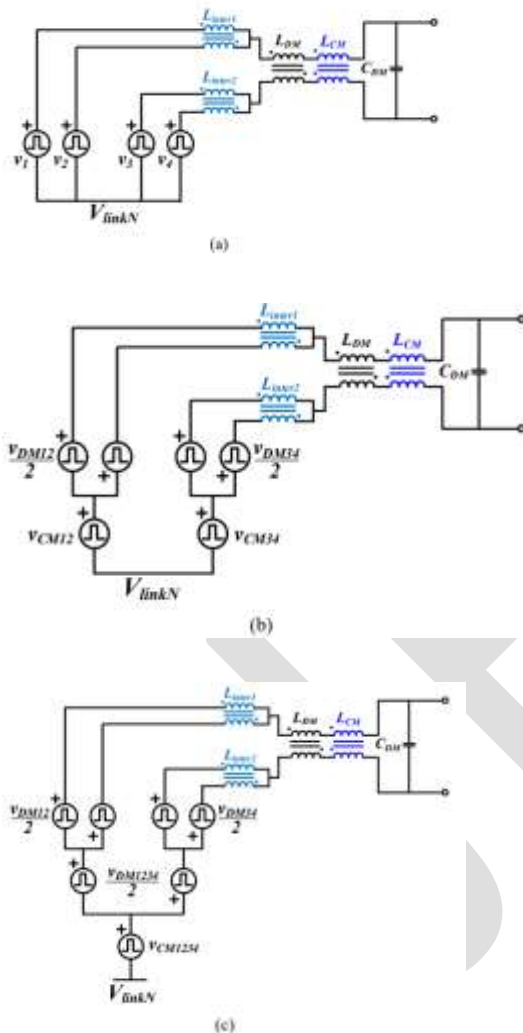


Fig. 9. Inductor voltage analysis. (a) Step 1 (b) Step 2 (c) Step 3

Since N_{Ac} and W_{Ac} are usually proportional to the volume, the volt-seconds on CM and DM components can be used to estimate their individual and total volume. Assuming the volt-seconds on the two interphase inductors are the same, the total inductor size for the circuit shown

in Fig. 8 can be expressed in (10) which includes two interphase inductors, one CM choke and one DM inductor.

$$Total\ volume \propto \frac{VS_{L_{inter}}}{B_{max1}} \times 2 + \frac{VS_{L_{CM}}}{B_{max2}} + \frac{VS_{L_{DM}} \cdot I_{max}}{B_{max3} \cdot \Delta I_{max}}$$

In this equation, VSLinter, VSLCM, VSLDM are the maximum volt-seconds on the interphase inductor, CM choke and DM inductor. Bmax1, Bmax2, and Bmax3 are the allowed maximum flux density for the core material of each component, and they are assumed to be the same since the same core material is used in this design. It can be observed that the volt-second on DM inductor has a coefficient of $I_{max}/\Delta I_{max}$, which is the ratio between the maximum inductor current and the maximum

inductor ripple current. Its value is usually between 5 and 20 which corresponds to 20% and 5% ripple current. This gives the DM inductor a high weighting factor in the total volume.

Analysis of the voltage on each inductive component To simplify the volt-second calculation of each component, the phase-legs are replaced with equivalent DM and CM voltage sources. In Fig. 9(a), the four phase-legs in Fig. 8 are replaced with controlled pulsating voltage sources v1, v2, v3 and v4 without switching cycle average. VlinkN is the voltage of the dc link negative rail.

It is worth noting that these equations are only valid for switching cycle volt-second analysis. The voltage appearing on the ac port will also influence the voltage waveform on LDM. However, since this voltage changes at 50 or 60 Hz, it will not influence the switching cycle flux swing calculation. In addition, the voltage applied on LCM could be smaller than the calculated value depending on how the power stage is grounded. However, this equation shows the worst case where all the voltage is applied on LCM. If LCM is designed based on this criterion, it can work with flexible grounding schemes. In general, the four interleaved phase-legs can be divided into two groups. In Fig. 8, the interleaved phase-legs s1 and s2 are in one group; s3 and s4 are in the other group. Within each group, the two phase-legs are connected through an interphase inductor and share the same duty cycle. If the duty cycles are considered symmetric around 0.5 for the two groups, i.e., the duty cycles are $0.5 + d/2$ and $0.5 - d/2$ respectively, then the sum of

the two duty cycles is always equal to one. When the two groups of phase-legs are not phase shifted, the PWM signals for the upper switches of the four phase-legs during one switching cycle are shown in Fig. 10. The driving signals for the lower switches are complementary to the upper.

5. EXPERIMENTAL RESULTS

Under interleaving, the converter requires a total of eight phase-legs. The concept of modular design is adopted to achieve better maintainability and scalability. A pluggable phase-leg card is designed as the basic unit to construct the converter. Fig. 32 shows the structure of a single phase-leg card. Two isolated power supplies and gate drivers are included in each card for the upper and lower MOSFETs. The gate driver ICs accept the PWM signals from the controller and drive the MOSFETs. The card also includes desaturation protection for over-current and active clamping to prevent the false turn-on during switching transient. When an error occurs, the protection circuit turns off the driving signals immediately and issues a fault signal to notify the controller. A few small decoupling capacitors are put near the MOSFETs to minimize the switching power loop and reduce the voltage overshoot during the device turning-off. Fig. 33 shows the printed circuit board (PCB) design of the phase-leg card. The gate drivers and power supplies are placed on the front side of the PCB while two MOSFETs in TO-247 package are attached to the heat sink and placed on the back side. It is important to minimize the device driving loop, as shown by the orange loop. The gate drivers are put

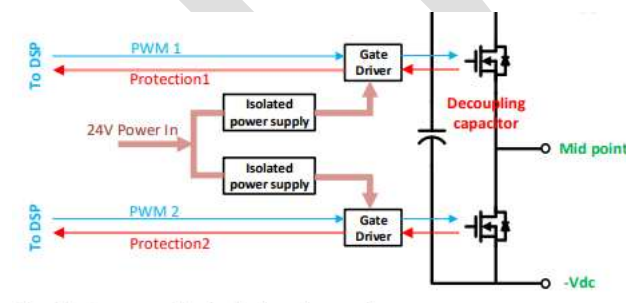


Fig 10. Structure of a single phase-leg card.

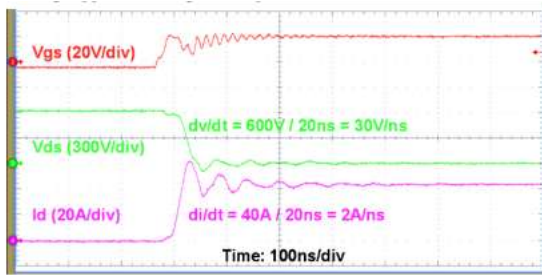


Fig. 11. MOSFET turn-on waveforms.

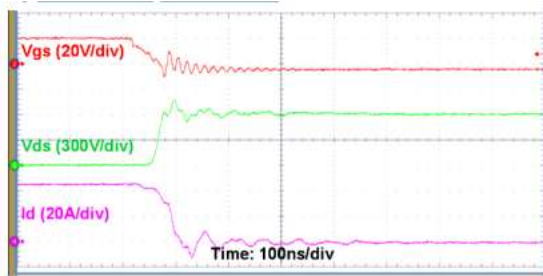


Fig. 12. MOSFET turn-off waveforms.

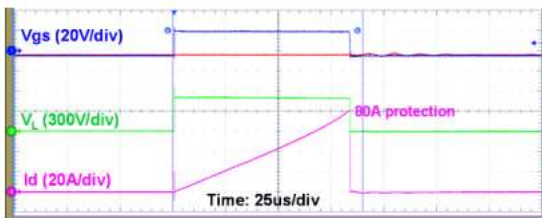


Fig. 13. Desaturation/over-current protection test.

very close to the device with gate resistor R_g and decoupling capacitors $C_{decouple}$. If the loop covers a large area, the parasitic inductance causes gate voltage overshoot or undershoot, which may falsely turn on the device or damage the device gate terminal. The signal and power terminals are arranged at the bottom of the card. The thicker pins are for power transmission and the thinner pins are for the PWMs and fault signals. The phase-leg card is tested under nominal voltage and current by double pulse testing. Fig. 34 and Fig. 35 show the magnified waveforms for the turn-on and turn-off transients with a 5.1Ω gate resistor. In the graph, V_{gs} is the gate-to-source voltage, V_{ds} is the drain-to-source voltage, and I_d is the drain current. The switching

dv/dt is 30V/ns and the di/dt is 2A/ns during the turn-on transient. The gate voltage and drain voltage have some ringing but the magnitude is well within the MOSFET rating

6. CONCLUSION

A converter topology with its filter and controller design are discussed to satisfy the demand for interconnecting 380 V bipolar dc microgrids and the single-phase ac utility. The twostage full-bridge topology reduces the required double-line frequency capacitors and attenuate the CM coupling between the grounded ac and dc systems. Both the interleaving of SiC MOSFETs and adaptive dc-link voltage control are effective approaches to improve the converter efficiency. The voltsecond applied on each inductive component is a good indicator to estimate the size and assist the magnetics design. By choosing different interleaving angles, volt-seconds and volumes of different inductive components change with different trends which requires a system optimization to achieve the minimized total volume. Pluggable phase-leg module design has the advantages of better maintainability and scalability. A 10 kW converter prototype is built using developed modules and achieves an efficiency $> 97\%$ under a wide load range. Lastly, the CM voltage on the dc bus is controlled by incorporating a CM voltage controller to the full-bridge dc-dc stage. The control loop transfer function is similar to a buck converter, so the compensator design is straightforward after identifying the values of critical components. With the decoupled topology and CM controller, the dc bus voltages are symmetric to the ground without any ripple.

REFERENCES

- [1] A. Sannino, G. Postiglione, and M. H. J. Bollen, "Feasibility of a DC network for commercial facilities," *IEEE Trans. Ind. Appl.*, vol. 39, no. 5, pp. 1499–1507, Sep. 2003.
- [2] D. Salomonsson and A. Sannino, "Low-Voltage DC Distribution System for Commercial Power Systems With Sensitive Electronic Loads," *IEEE Trans. Power Deliv.*, vol. 22, no. 3, pp. 1620–1627, Jul. 2007.
- [3] D. Boroyevich, I. Cvetković, D. Dong, R. Burgos, F. Wang, and F. Lee, "Future electronic power distribution systems a contemplative view," in *Optimization of Electrical and Electronic Equipment (OPTIM)*, 2010 12th International Conference on, 2010, pp. 1369–1380.

- [4] H. Kakigano, Y. Miura, and T. Ise, "Low-Voltage Bipolar-Type DC Microgrid for Super High Quality Distribution," IEEE Trans. Power Electron., vol. 25, no. 12, pp. 3066–3075, Dec. 2010.
- [5]. G. Jagga Rao, Y. Chalapathi Rao " Artificial Intelligence & Machine Learning Based Wireless MIMO-OFDM Communication system in JAG6G Analysis "in Volume 8-Issue 4, pp. 3740-3755, May2019.
- [6]. G. Jagga Rao, Y. Chalapathi Rao, Dr. Anupama Desh Pande "A Novel Approach for High Secured Image Transmission in 6G via MIMO-OFDMA process in NCHAOS Encryption Algorithm" in Volume 9-Issue 10, pp. 1481-1492, Oct 2019.
- [7]. G. Jagga Rao, Y. Chalapathi Rao, Dr. Anupama Desh Pande "Detection For 6G-NOMA Based Machine Learning Optimization for Successive Adaptive Matching Pursuit Analysis", Q3, pp. 1803-1812, Jan 2020.
- [8]. Sudha, Y. Chalapathi Rao, G. Jagga Rao " Machine Learning based Copy-Move Forgery Detection with Forensic Psychology Ultra-Hd images "in Volume 81, Nov-Dec-2019.
- [9]. Dr. B Sankara Babu, Srikanth Bethu, K. Saikumar, G. Jagga Rao, "Multispectral Satellite Image Compression Using Random Forest Optimization Techniques" Journal of Xidian University, in Volume 14, Issue 5-2020.
- [10]. G. Jagga Rao, Y. Chalapathi Rao, "Human Body Parts Extraction in Images Using JAG-Human Body Detection (JAG-HBD) Algorithm Through MATLAB" Alochana Chakra Journal, Volume IX, Issue V, May/2020.
- [11]. Dr. k. Raju, A. Sampath Dakshina Murthy, Dr. B. Chinna Rao, G. Jagga Rao "A Robust and Accurate Video Watermarking System Based On SVD Hybridation For Performance Assessment" International Journal of Engineering Trends and Technology (IJETT) – Volume 68 Issue 7 - July 2020.
- [12]. G. Jagga Rao, Y. Chalapathi Rao, Dr. Anupama Desh Pande "A Study of Future Wireless Communication: 6G Technology Era " volume 14, issue 11,2020.

- [13]. G. Jagga Rao, Y. Chalapathi Rao, Dr. Anupama Desh Pande "Deep Learning and AI-Based millimeter Wave Beamforming Selection for 6G With Sub-6 GHz Channel Information" Volume 21 : Issue 11 – 2020.
- [14]. G. Jagga Rao, Y. Chalapathi Rao, Gopathi Shobha, G. Jagga Rao, P. Lavanya, M. Ravi "Deep Learning based Millimeter Wave/Sub - THz RMIMO-OFDM Systems with Beamforming Wireless communication " International Journal of Membrane Science and Technology, 2023, Vol. 10, - 2023.
- [15] L. C. Breazeale and R. Ayyanar, "A Photovoltaic Array Transformerless Inverter With Film Capacitors and Silicon Carbide Transistors," IEEE Trans. Power Electron., vol. 30, no. 3, pp. 1297–1305, Mar. 2015.
- [16] B. N. Alajmi, K. H. Ahmed, G. P. Adam, and B. W. Williams, "SinglePhase Single-Stage Transformer less Grid-Connected PV System," IEEE Trans. Power Electron., vol. 28, no. 6, pp. 2664–2676, Jun. 2013.
- [17] R. Gonzalez, E. Gubia, J. Lopez, and L. Marroyo, "Transformerless Single-Phase Multilevel-Based Photovoltaic Inverter," IEEE Trans. Ind. Electron., vol. 55, no. 7, pp. 2694–2702, Jul. 2008.
- [18] L. Zhang, K. Sun, Y. Xing, and M. Xing, "H6 Transformerless FullBridge PV Grid-Tied Inverters," IEEE Trans. Power Electron., vol. 29, no. 3, pp. 1229–1238, Mar. 2014.
- [19] Y. Tang, W. Yao, P. C. Loh, and F. Blaabjerg, "Highly Reliable Transformerless Photovoltaic Inverters With Leakage Current and Pulsating Power Elimination," IEEE Trans. Ind. Electron., vol. 63, no. 2, pp. 1016–1026, Feb. 2016.
- [20] K. Mainali and R. Oruganti, "Conducted EMI Mitigation Techniques for Switch-Mode Power Converters: A Survey," IEEE Trans. Power Electron., vol. 25, no. 9, pp. 2344–2356, Sep. 2010.
- [21] M. Cacciato, A. Consoli, G. Scarcella, and A. Testa, "Reduction of common-mode currents in PWM inverter motor drives," IEEE Trans. Ind. Appl., vol. 35, no. 2, pp. 469–476, Mar. 1999.

- [22] M. C. Cavalcanti, K. C. de Oliveira, A. M. de Farias, F. A. S. Neves, G. M. S. Azevedo, and F. C. Camboim, “Modulation Techniques to Eliminate Leakage Currents in Transformerless Three-Phase Photovoltaic Systems,” *IEEE Trans. Ind. Electron.*, vol. 57, no. 4, pp. 1360–1368, Apr. 2010.
- [23] C. C. Hou, C. C. Shih, P. T. Cheng, and A. M. Hava, “Common-Mode Voltage Reduction Pulsewidth Modulation Techniques for Three-Phase Grid-Connected Converters,” *IEEE Trans. Power Electron.*, vol. 28, no. 4, pp. 1971–1979, Apr. 2013.
- [24] J. D. Kagerbauer and T. M. Jahns, “Development of an Active dv/dt Control Algorithm for Reducing Inverter Conducted EMI with Minimal Impact on Switching Losses,” in 2007 IEEE Power Electronics Specialists Conference, 2007, pp. 894–900.