A 12-BIT COLUMN-PARALLEL TWO-STEP SINGLE-SLOPE ADC WITH A FOREGROUND CALIBRATION FOR CMOS IMAGE SENSORS

Radhika Rayeekanti , AssociateProfessor, ECE department, Bhoj Reddy Engineering College for Women, Hyderabad, TS
Suchithra Parvathaneni and Sridurga Pulagam as UG SCHOLARS, ECE department, Bhoj Reddy Engineering College for Women, Hyderabad, TS.

Abstract: A novel 12-bit column-parallel two-step single-slope (SS) analog-to-digital converter (ADC) for high-speed CMOS image sensors. A CMOS image sensor, short for Complementary Metal-Oxide-Semiconductor image sensor, is a tiny electronic device that plays a crucial role in capturing the images we see on our digital cameras, smartphones, and various imaging devices. It acts as the "electronic eye" of these devices, converting light into digital information we can process and view.Cooperating with the output offset storage (OOS) technique, a new correlated double sampling (CDS) is adopted to reduce the non-uniformity in column-level ADCs. In the proposed structure, the decision point of the comparator is independent of the input signal. The variation of the comparator offset caused by the input level is eliminated. Through a foreground calibration, the non-idealities from the ramp generator and the column ADC are both corrected.

The ADC uses a two-step conversion process. The conversion is split into two phases: a coarse conversion and a fine conversion. This two-step approach allows for faster conversion times compared to traditional single-slope ADCs.

Design and simulation in a 130nm CMOS process, the proposed ADC achieves the differential non-linearity (DNL) of +0.76/−0.8 LSB and the integral non-linearity (INL) of +1.06/−0.84 LSB at a sampling frequency of 100 KS/s with the calibration. The effective number of bits (ENOB) is also improved from 4.66 bits to 11.25 bits. The single ADC occupies an active area of 7.5 × 775 μm2 and the power consumption is 72 μW.

Introduction

CMOS Image Sensor (CIS) is an essential visual system component used in DSLR cameras, digital camcorders, and medical equipment.CMOS Image Sensor is a "electronic eye" semiconductor device. As digital imager technology advances, demand for CMOS imagers with high resolution format, frame rate, and ADC resolution has increased significantly.The working idea of a CMOS image sensor was proposed in the late 1960s, but microfabrication technology evolved sufficiently to commercialize the device in the 1990s. CCD or CMOS image sensors are used in most digital cameras and mobile phones.CCD and CMOS are semiconductor "electronic eyes." They both employ photodiodes but have different manufacturing and signal reading methods. CCD sensors were dominating because to their greater sensitivity and image quality, but CMOS sensors began to outsell CCD sensors in 2004.A charge-coupled device (CCD) image sensor includes capacitors with electric

charges matching to pixel light intensity. A control circuit transfers each capacitor's contents to its neighbor, and the array's final capacitor discharges its charge into a charge amplifier. CCD sensors convey data bucket-brigade-style. A complementary metal oxide semiconductor (CMOS) image sensor amplifies pixel signals independently using a photodiode and CMOS transistor switch for each pixel. The matrix of switches allows direct, sequential access to pixel signals at a faster rate than a CCD sensor. An amplifier for each pixel decreases noise while reading electrical signals produced from collected light.Pixel size has decreased from 10-20 micron large pixels in the mid-1990s to 6-8 micron sensors on the market today. Demand for tiny electronic image equipment like surveillance and telephone cameras has driven designers to reduce pixel sizes. Image sensors with 4-5 micron pixels are used in smaller arrays, while multi-megapixel circuits will need 3–4 micron pixels. CMOS image sensors must be made on 0.25-micron or thinner lines to meet these requirements. If scaling ratio factors approach unity, smaller line widths may cram more transistors into each pixel element while preserving fill factors. Advanced technologies including in-pixel analog-to-digital converters, full-color processing, interface logic, and other complicated circuitry designed to maximize CMOS sensor flexibility and dynamic range should be viable with 0.13 to 0.25-micron production lines.As market demand grows, more CMOS fabrication units are incorporating color filters and microlens arrays for image sensor manufacture. Image-critical optical packaging requires clean rooms and flat-glass handling equipment not found in logic and processor integrated circuit manufacturers. Thus, image sensor manufacturing ramp-up costs might be high.CMOS image sensors are cheaper to make than CCD ones because semiconductor manufacturing equipment may be reused. CMOS sensors consume less power and have less blur and blooming than CCD sensors, which utilize high-voltage analog circuits. CMOS sensors with an on-chip image processing circuit are being developed for image recognition and artificial vision because logic circuitry can be integrated onto the chip during manufacture. Some devices are currently in use.

This boosts column ADC conversion speed. Thus, successive approximate register (SAR), cyclic, and single-slope (SS) column-parallel ADC designs have been used to enhance sampling rate. SAR ADCs are used in high-speed image sensors, however their DAC capacitor array takes up a lot of silicon. Cyclic ADCs use less silicon while maintaining SAR ADC speed. They need more power due to the high-gain and high-speed operating amplifier. CIS uses SS ADCs due of their simplicity, low power dissipation, great linearity, and compact space. Slow conversion speed of SS ADCs. T-bit SS ADCs take 2T clock cycles, which is longer than SAR and cyclic ADCs. Several high-speed SS ADCs have been documented, however their high clock frequency consumes power.

We suggest several two-step (TS) SS ADCs to solve the low-speed issue. T-bit TS SS ADCs convert A/D into M-bit coarse and N-bit fine conversions, where T = M + N. TS-SS ADC conversion time is lowered to 2M + 2 N clock steps, improving conversion speed compared to normal SS ADC. A holding capacitor stores the final analog coarse voltage. But parasitic capacitors in the holding capacitor will distort the fine ramp slope. Using a four-input comparator, the coarse and fine ramp conversion routes are separated. While it preserves the fine ramp slope, signal-dependent charge injection reduces ADC linearity.

This design performs two-step conversion without memory capacitors by connecting coarse ramp reference voltages to comparator input nodes. However, the comparator's input routes expand exponentially with coarse conversion resolution. Routing will get more difficult and switch faults will increase. Even if TS-SS ADCs are

implemented in various circuit topologies, the signal-dependent comparator offset will reduce their linearity. A unique 12-bit two-step SS ADC is proposed here. Merging the sampling and conversion routes removes the dynamic comparator offset. A foreground calibration allows the proposed TS-SS ADC to convert at fast speed with outstanding linearity.

TWO-STEP ADC

A multistage comparator, sampling capacitor (CS), holding capacitor (CH), switches, delay control circuitry, and data memory boost each amplifier's strength by 17 dB, 17 dB, and 62 dB, respectively, in the proposed column ADC. The PreAmp1 and PreAmp2 noise contributions must be included as the gain of the preAmp1 is only 1. OOS (auto-zeroing) shapes preAmp1 input-referred noise using a comb filter. Low-frequency noise is reduced. The simulation indicates that preAmp1 and preAmp2 have input-referred noises of 49 and 36 μVrms, respectively. Simplified multistage comparator schematic.The proposed column ADC comprises four primary operations: reset sampling, signal sampling, coarse A/D conversion, and fine A/D conversion. Reset Sample. CS samples the pixel reset voltage Vreset with switches RX, SS, SH, SR, and SA closed. Then, when the switch RX is off, the error the resistor DAC-based ramp generator, shared by all column ADCs, has two parts: a coarse ramp VRC for M-bit coarse conversion and a fine ramp VRF for N-bit fine conversion. The CS samples the reset and signal voltages from 4-T APS, giving the intended ADC T = M + N bit resolution. CH is series-connected to ramp generator. In coarse conversion, the CH top plate stores the final charge. This charge is coarse conversion residue. Fine conversion is achieved by driving the CH bottom plate with the fine ramp. Delay control logic reduces coarse conversion judgment error. Column memory caches conversion results. The common-mode voltages of the PreAmp1 and PreAmp2 are 1.6 V and 0.8 V, respectively. A multistage comparator architecture with output offset storage (OOS) was employed to reduce pixel offsets during CDS. Due to its single-ended construction, the preAmp1's input swing must encompass the analog input signal's range for proper conversion. Thus, the preAmp1 uses PMOS transistors for input pairs and 3.3 V for supply. PreAmp1 gain is adjusted to 1 to avoid saturation of its output. The direct-current (DC) split of the offset storage capacitor CD allows other pre-amplifiers to use 1.2V supplies to save electricity. CS samples the NMOS input pairs voltage VE from RX, including charge injection and clock feed through, from preAmp2 to preAmp4 after a delay. Next, successively turning off SR and SS eliminates sampling switch SS-induced signal-dependent switch faults. Finally, the coarse ramp switch SC loads the coarse ramp's maximum voltage VCT into the CS's left plate (voltage node P2). The comparator VP1 positive input voltage is,

$$V_{P1} = V_{CM1} - (V_{reset} + V_E - V_{CT})$$

where V_S is the actual signal that corresponds to the incident light intensity. Then, S_C is open and S_R, S_S are closed. The signal voltage V_{signal} is sampled by C_S. Next, similar to the reset sampling phase, the SR is turned off before the S_S. Coarse A/D conversion. With the closure of the S_C, the left plate of the C_S is driven by the coarse ramp V_{RC}. Considering the stored charge on the C_D, the equivalent voltage at the input node P_1 is calculated from ,

$$V'_{P1} = V_{CM1} + (V_S - (V_{CT} - V_{RC})).$$

The input offset of the preAmp1, the reset signal from the pixel, and the charge errors from the R_X are all canceled. Hence, with the output coupling capacitor C_D, the C_{DS} operation based OOS is realized. The

essence of the conversion is to determine the sign of $V'_{P1} - V_{CM1}$. During the coarse A/D conversion, V_{RC} starts in synchrony with the coarse counter and sweeps from V_{CT} to $V_{CT} - V_{FS}$, where V_{FS} is the fullscale voltage. If the signal V_S is,

$$V_{CM1} + (V_S - (m + 1)\ (V_{RC})') < V_{CM1} < V_{CM1} + (V_S - m\ V'_{RC}),$$

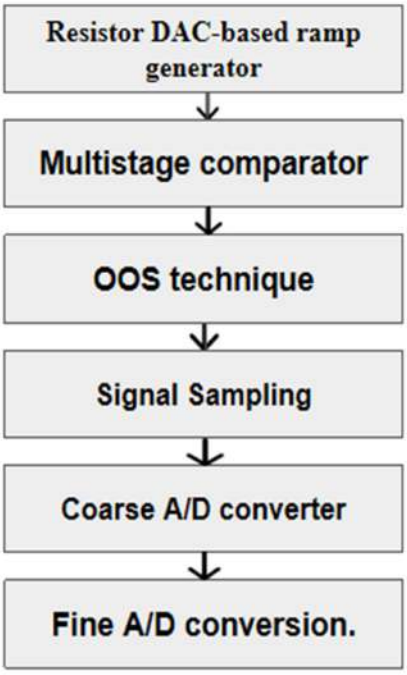


Fig.2.1 Block Diagram of the proposed Two Step SS ADC

The comparator output *VO* will be changed to the logic low when $V_{CT} - V_{RC}$ becomes (m + 1) V'_{RC}. V'_{RC} is the minimum conversion voltage of the coarse ramp, which is $V_{FS} / 2M$. Then, the upper *M*-bit memory stores the coarse counter value as the coarse A/D result D_M and S_H is turned off. At this moment, the bottom plate charge of the CH (node P_3) is,

$$Q_{CH} = V_{ref} - (V_{CT} - (m + 1)\ V'_{RC})\ \times C_D$$

When *VRC* drops to $VCT - VFS$, the coarse conversion is over and the SC is open. Fine A/D conversion. When SF is closed, the fine ramp signal *VRF* is coupled to the positive input of the comparator through the CH. According to the charge conservation, the equivalent voltage at the input node P1 is obtained from ,

$$V'_{P1} = V_{CM1} + (V_S - (m + 1)\ C') + V_{RF} - V_{ref}$$

where $V_{RF} - V_{ref}$ is the effective fine ramp voltage. Since the fine ramp signal V_{RF} spans from $V_{ref} + V'_{RC}$ to V_{ref} , the variation of the resulting coupling voltage V'_{P1} is V'_{RC}. The step of the fine ramp is $V'RF$, which is

$V'RC/2N$. When V'_{P1} drops below the V_{CM1}, the comparator output VO is changed to the logic low again and the lower N-bit memory stores the fine counter value as the fine A/D result D_N . Therefore, the final digital output D_{OUT} is calculated from:

$$D_{OUT} = 2\,N \times D_M + D_N - 2\,N$$

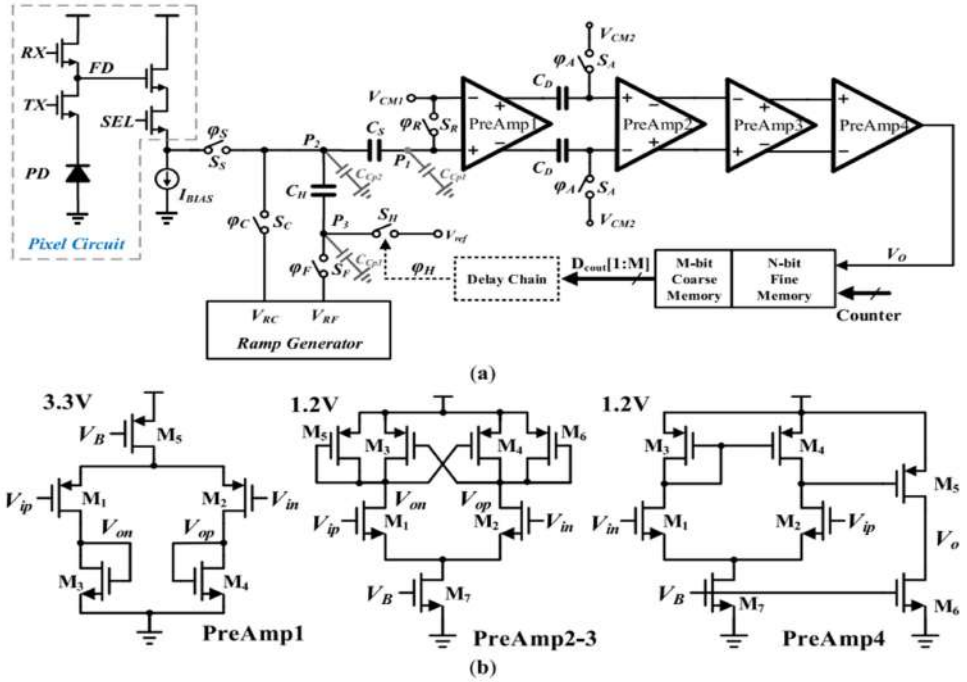


Figure.2.2 Simplified schematics of (a) the proposed two-step SS ADC with the 4 T-APS and (b) the multistage comparator

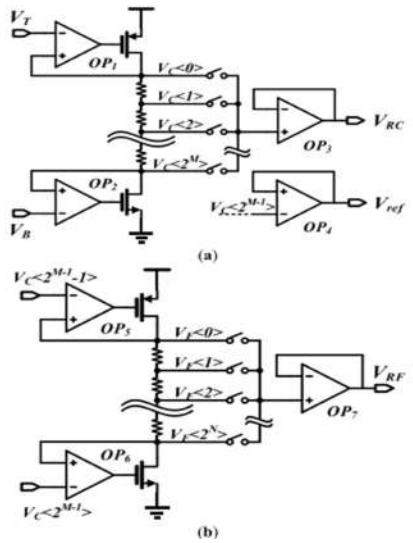


Figure 2.3: Simplified schematics of the ramp generator. (a) Coarse Ramp (b) Fine Ramp

ACCURACY CONSIDERATION

Overall, ramp generator linearity determines column ADC performance. The ramp generator uses the resistor

string DAC (RDAC) design to ensure ADC monotonicity. For high-resolution applications (beyond 10-bit), voltage selector switch components expand exponentially with bits. Larger RC output delay, inadequate silicon area, and difficult metal routing will occur. The resistor-resistor-string DAC (RRDAC) is used with two cascaded resistor strings.

The reference buffers (OP5 and OP6) link the fine resistor ladder to a unit coarse resistor. The fine ladder does not lower the unit coarse resistor's effective resistance since the op-amps are isolated. The on-resistance of the voltage selection switches cannot lower the effective resistance of the unit coarse resistor since the input nodes of the output buffers OP3 and OP4 have high input impedance. Switch mismatches hardly affect ramp generator linearity. Since ramp generator voltage lowers monotonically, only one pair of switches is switched every conversion interval. One switch is on, one off. Clock feed-through faults will be minimized and gone quickly. The RRDAC's main errors are resistor mismatch and amplifier offsets. To examine how resistor mismatch affects ADC performance, we simulated averaged ENOB and SFDR as a function of mismatch deviation σ(1 R/R). As resistor mismatch rises, column ADC linearity deteriorates. ENOB and SFDR are 9.42 bits and 62.27 dB with 1% mismatch variation.

In fact, op-amp input-referred offsets reduce ADC performance. The fine conversion changes the CH bottom plate from Vref to VRF. OP4 and OP7's offset difference Vdiff shifts the effective fine ramp vertically. Digital output will have a dead-band from the over-ranged ramp. After considering the offsets in OP5 and OP6, the effective fine ramp conversion range and ramp slope change. Shadows show the likely range of the true effective fine ramp induced by OP5 and OP6 offsets.

In the column ADC, non-idealities such as charge errors of MOS switches, parasitic capacitors, and comparator offsets can also make the proposed structure malfunctioned. After the reset sampling phase, taking into account these non-ideal

factors, the resulting positive input voltage V_{P1} is rewritten with ,

$$V_{P1} = V_{CM1} + \frac{Q_{SR}}{C_S + C_{Cp1}} - \frac{C_S}{C_S + C_{Cp1}}\left(V_{reset} + V_E - \left(V_{CT} + V_{RC,offset}\right)\right)$$

where $V_{RC,offset}$ is the output offset of the coarse ramp, Q_{SR} is the charge error when S_R is open, C_{Cp1} is a parasitic capacitor existing at node P_1.

Similarly, when the signal sampling is over and the coarse conversion began, the equivalent voltage V'_{P1} is re-calculated from,

$$V'_{P1} = V_{CM1} + V_{offsetr} + \frac{\Delta Q_{SA}}{C_D} - \frac{C_S}{C_S + C_{Cp1}}\left(V_S - (V_{CT} - V_{RC})\right),$$

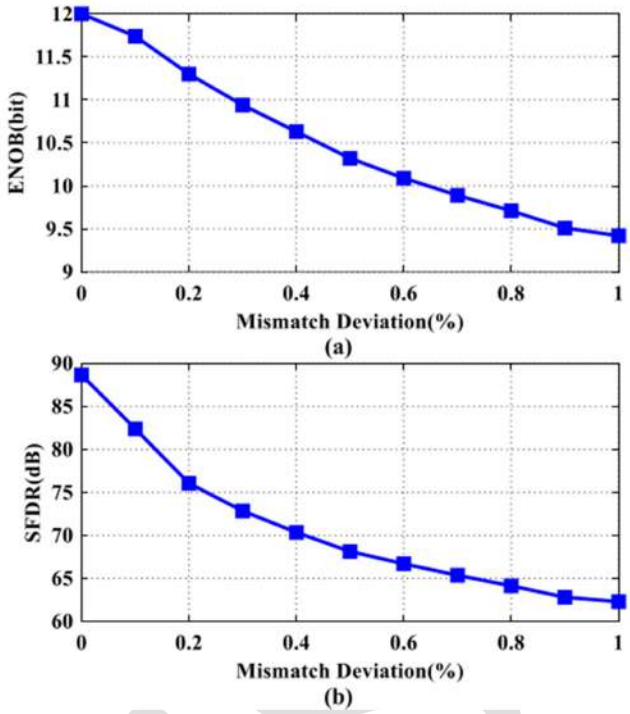


Figure 3.1: The dynamic performance versus mismatch deviation. (a) ENOB; (b) SFDR

where $V_{offsetr}$ is the residual input-referred offset contributed by preAmp2-4. Q'_{SA} is the mismatch in charge injection from two switches S_A. Thanks to the C_{DS}, the output offset $V_{RC,offset}$ of the coarse ramp and the charge error Q_{SR} are both canceled. When the comparator output VO is changed to the logic low, SH is switched off immediately and the charge error QSH injects into the bottom plate of the C_H. After V_{RC} drops to $V_{CT} - V_{FS}$, the SC is open and the charge error Q_{SC} flows into the node P_2. During the fine A/D conversion, the equivalent voltage V'_{P1} is re-calculated from,

$$
\begin{aligned}
V'_{P1} &= V_{CM1} + V_{offsetr} + \frac{\Delta Q_{SA}}{C_D} \\
&\quad - \alpha\left(V_S + f\left(V_{RC}\right) - V_{CT}\right. \\
&\quad \left. + \beta\left(V_{RF} - V_{ref}\right) + V_{E,SW}\right), \\
f\left(V_{RC}\right) &= \beta\gamma V_{RC} + (1 - \beta\gamma)\left(V_{CT} - V_{FS}\right), \\
\alpha &= \frac{C_S}{C_S + C_{Cp1}}, \quad \beta = \frac{C_H}{C_H + C_{Cp2} + \left(C_S \| C_{Cp1}\right)}, \\
\gamma &= \frac{C_H}{C_H + C_{Cp3}}, \quad V_{E,SW} = \frac{\beta Q_{SC}}{C_H} - \frac{\beta\gamma Q_{SH}}{C_H}
\end{aligned}
$$

Here C_{Cp2} and C_{Cp3} are parasitic capacitors existing at nodes P_2 and P_3 ,respectively. VE , SW is the switch error caused by S_C and S_H .

The parasitic capacitors will cause a severe ramp error, which degrades the linearity of the proposed ADC. The effective coarse ramp voltage used for fine conversion is no longer the original coarse ramp V_{RC} but the f (V_{RC}). The variation in the coarse ramp slope will cause a huge voltage gap such as V_D, which is far beyond the conversion range of the fine ramp. For example, when V_{RC} drops to V_{H2} and S_H is open at the time of T_2, the resulting voltage at the node P_1 is V_H instead of V_{H2}. To eliminate this voltage gap, the switch SH needs to be turned off in advance at the time of T_1.

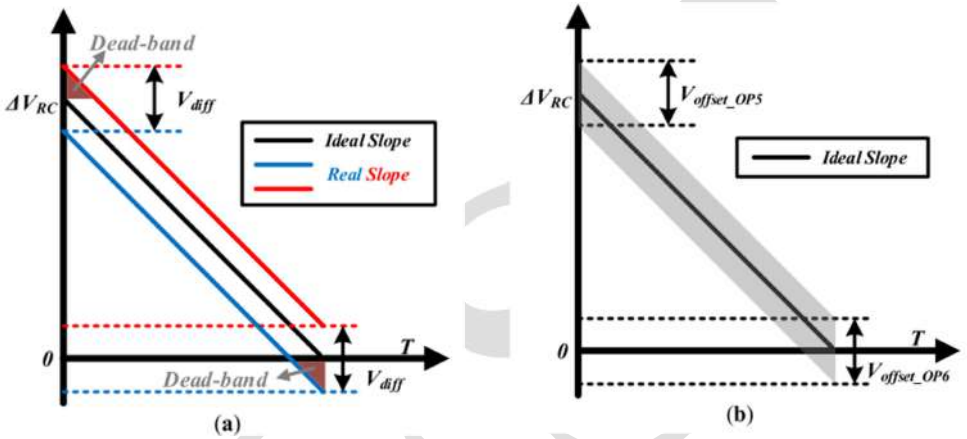


Figure 3.2: The degradation of the effective fine ramp are caused by (a) offsets of OP4 and OP7, and (b) offsets of OP5 and OP6

However, for a causal system, it cannot be implemented physically. If V_{RC} drops to $V_{CT} - V_{FS}$, V_{RC} will be reset to V_{CT} subsequently. After that, S_C will be open. The resulting effective coarse ramp is changed to,

$$f(VRC) = \beta\gamma\ VRC + (1 - \beta\gamma)\ VCT,$$

The calibrated coarse ramp is the vertical shift of the real ramp. To ensure that the voltage used in the fine conversion is V_{H2}, the opening time of the S_H is simply delayed by T_D. Therefore, by constructing a proper delay chain and expanding the range of coarse ramp signal (V_{Re}), this coarse ramp error can be alleviated. However, there is also a serious slope difference between the effective coarse ramp and the effective fine ramp.

The slope of the effective coarse ramp and the effective fine ramp are denoted as $\beta\gamma$ and β, respectively. Since the input common-mode voltage V_{CM1} is kept at the same level during the whole conversion process, the decision point of the comparator is independent of the input signal. The variation of comparator offset caused by the input level can be canceled. The residual input-referred offset $V_{offsetr}$ is viewed as a constant static voltage. Since switches SC, SH, and SA are all connected to fixed voltages, the resulting charge errors Q_{SC}, Q_{SH}, and Q'_{SA} are also regarded as static errors when these switches are turned off. Hence, the above static errors from the column ADC can be corrected by a foreground calibration, as depicted.

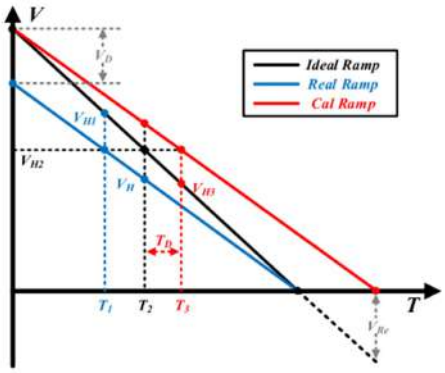
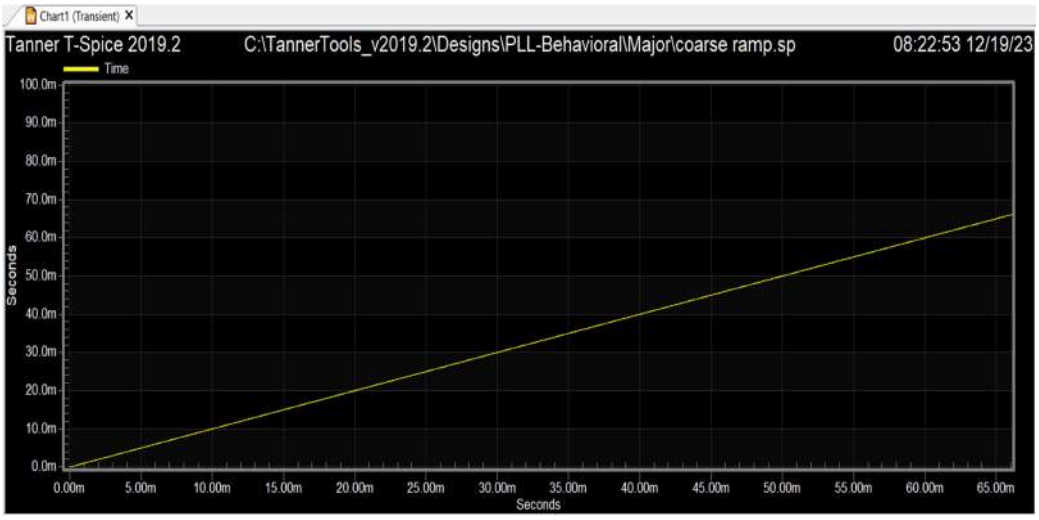


Figure 3.3: The degradation of the effective coarse ramp

Since the residual comparator offset $V_{offsetr}$ and charge error Q'_{SA} exist in the whole conversion, they cannot introduce the extra conversion dead-band. However, charge errors Q_{SC}, Q_{SH} only exist in the fine conversion, they also cause the vertical shift of the effective fine ramp. Thus, the deadband in digital output is also generated.

RESULT

The primary result of the ADC is the digital representation of the converted analog signal of the fine and coarse ramp generator output.



(a)

(b)

Figure 8.1: (a) Timing diagram of the coarse conversion ramp (b) Timing diagram of the fine conversion ramp

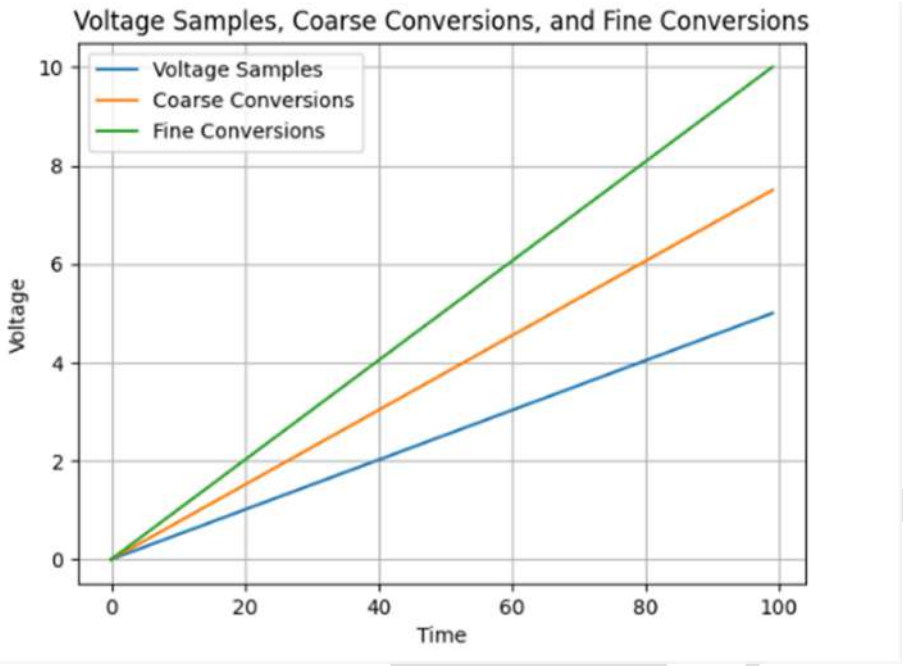


Figure 8.2: Ramp Generated after Foreground Caliberation

A behavioral model of the proposed ADC is created in Matlab, and the simulation accounts for the resistor mismatch, the parasitic capacitors, the charge injection and feed through of the non-ideal MOS switches, the offsets of the reference op-amps, and the comparator offset and noise. In the 130 nm CMOS process, the resistor variation σ(1 R/R) is 1%. Due to the usage of the metal-oxide-metal (MOM) capacitor, the percentages of top- and bottom-plate parasitic capacitance of the corresponding capacitors are both 3%. From the post-layout extraction, the parasitic capacitance caused by input pairs of the comparator is 25 fF. The standard deviations of the comparator offset and reference opamps offsets are all 7 mV. A total of 1000-runs Monte-Carlo simulation is done to estimate the non-linearity performance, as shown in Fig. 8.3. Since each calibrated weight of the coarse ramp is the accumulation of the resistor weights, the quantization error in each resistor weight will slightly degrade the linearity of the coarse ramp. For the dynamic performance, after the foreground calibration, the standard deviation (std) and average (mean) of ENOB are improved from 0.09/4.83 bits to 0.33/10.85 bits and the standard deviation and average of SFDR are improved from 2.71/39.92 dB to 4.09/72.03 dB. Because each resistor weight is correctly extracted, the deviation and average of maximum |DNL| are promoted greatly from 1.55/132.66 LSB to 0.12/0.7 LSB and the deviation and average of maximum |INL| are enhanced from 19.27/134.85 LSB to 0.59/1.84 LSB. With the foreground manner, the non-ideal errors of each ADC in the CIS can be corrected in sequence. It allows all column ADCs to share a global calibration engine, which greatly improves the area efficiency of the single ADC. For an ADC array with 1024 columns, the coarse calibration for the ramp offsets and the construction of the delay chain are both based on the first column. The delay latch array can also be shared by multiple columns to reduce the silicon area. Then, with a unified delay chain, the voltage information of the coarse ramp can be quantified in each ADC. Considering the size variation of MOS switches and the mismatch of comparator offsets, the static error weight W0 in each ADC needs to be measured and

stored. However, thanks to the different parasitic capacitors, the coarse ramp presents the different effective coarse weight in each ADC. For any original coarse ramp voltage VRC,i , there are 1024 corrected results due to 1024-column ADCs. It is impractical to store these results in memory, which causes a huge area dissipation. Hence, the column-to-column mismatch will be mitigated by an averaged operation. The fine calibration in each ADC is performed column by column, from ADC1 to ADC1024. The effective resistor weight W_{Ri} with the same sequence number i in different columns are accumulated until the correction of the last column is completed. Then, with the averaging operation, the unified weight information of resistors has been generated. Next, the weights of coarse ramp voltages are accumulated by each resistor weight. With the usage of the individual error weight W0 in each ADC and uniform coarse voltage weights, the area of memory is significantly reduced.

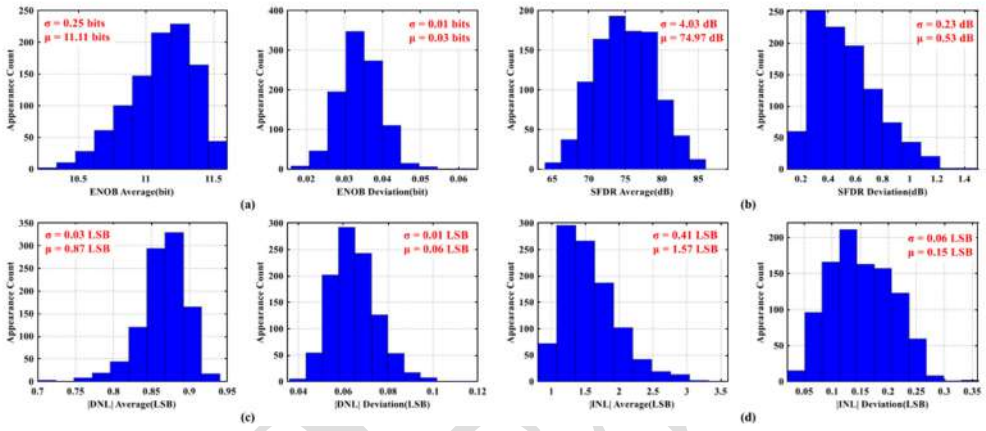


Figure 8.3: The performance distribution of the proposed ADCs array with the foreground calibration. (a) ENOB, (b) SFDR, (c) |DNL|, (d)|INL|

Similarly, the behavioral model of the ADCs array is also created in Matlab. The capacitance of the C_H and the C_S are implemented with 400 fF and 1 pF in the 130 nm CMOS process. The larger plate of the capacitor will cause a smaller capacitor mismatch σ(d(C)/C) of only 0.1%. The size variation of MOS transistors is 5%, resulting in different switch errors and parasitic capacitors. In each simulation, the performance of the ADCs array is calculated, which is the specification distribution (includes the average value μ and the standard deviation σ) of all column ADCs. With a total of 1000-runs Monte-Carlo simulation, the effect of the foreground calibration on the ADCs array is visualized in Fig. 8.3. Due to the weighted averaged operation, the quantization error that exists in each resistor weight will be weakened. Compared with the single ADC, the dynamic performance of the entire 1024-column ADC is slightly improved. The tiny performance deviation in Fig. 8.3 demonstrates the excellent consistency of the ADCs array with the proposed calibration.

The Performance is determined by ENOB, SFDR, |DNL|, |INL|. Effective Number of Bits (ENOB): ENOB represents the number of bits of an ideal ADC that would provide the same performance as the actual ADC under consideration. It quantifies the resolution of the ADC while accounting for noise and other imperfections.

$$ENOB = (SNR - 1.76) / 6.02$$

Where SNR is the Signal-to-Noise Ratio in dB. Spurious Free Dynamic Range (SFDR): SFDR is the ratio of the rms amplitude of the input signal to the rms amplitude of the largest spurious component. It indicates the dynamic range excluding distortion.

$$SFDR = 20 * \log10(V_{max} / V_{spurious})$$

Where V_{max} is the maximum output amplitude and $V_{spurious}$ is the amplitude of the largest spurious component. SFDR, SNDR, and ENOB are 35.31 dB, 29.84 dB, and 4.66 bits respectively before calibration. After foreground calibration. Dynamic performance improves with SFDR, SNDR, and ENOB reaching 78.55 dB, 69.49 dB, and 11.25 bits respectively after calibration. Monte Carlo analysis shows minimum ENOB and SFDR of 10.54 bits and 67.06 dB respectively, with maximum |DNL| and |INL| within 1 LSB and 4 LSB.

Differential Non-linearity (DNL): DNL is a measure of the variation from ideal step size between any two adjacent codes. It indicates the deviation of the actual step size from the expected value.

$$DNL = (V_{measured} - V_{ideal}) / V_{LSB}$$

Where $V_{measured}$ is the actual step size between two adjacent codes, V_{ideal} is the expected ideal step size, and VLSB is the voltage equivalent of the least significant bit. DNL peak error is +132.93/-1 LSB and after calibration DNL is reduced to +0.76/0.8 LSB.

Integral Non-linearity (INL): INL is the deviation of the actual transfer function from an ideal straight line. It represents the maximum deviation of any code from the ideal transfer function.

$$INL = \Sigma(DNL)$$

Where DNL is the Differential Nonlinearity. INL error is +18.6/-195.63 LSB without digital calibration and with calibration INL is significantly reduced to +1.06/-0.84 LSB.

CONCLUSION AND FUTURE SCOPE

Conclusions

A novel 12-bit column-parallel two-step single-slope (SS) analog-to-digital converter (ADC) for high-speed CMOS image sensors. Cooperating with the output offset storage (OOS) technique, a new correlated double sampling (CDS) is adopted to reduce the non-uniformity in column-level ADCs. In the proposed structure, the decision point of the comparator is independent of the input signal. The variation of the comparator offset caused by the input level is eliminated.DNL) of +0.76/−0.8 LSB
and the integral nonlinearity (INL) of +1.06/−0.84 LSB at a sampling frequency of 100 KS/s with the calibration. The effective number of bits (ENOB) is also improved from 4.66 bits to 11.25 bits. The single ADC occupies an active area of 7.5 × 775 μm2 and the power consumption is 72 μW. The use of a foreground calibration approach allows for adaptability to changes in environmental conditions or aging effects, ensuring the long-term reliability and stability of the ADC. In the column ADC, non-idealities such as charge errors of MOS switches, parasitic capacitors, and comparator offsets can also make the proposed structure malfunctioned. Similarly, to calibrate the slope degradation of the coarse ramp caused by parasitic capacitors, the range of the original coarse ramp is also slightly extended analyzed. Through a foreground calibration, the non-idealities from the ramp generator and the column ADC are both corrected and also to minimizing power consumption by continuously correcting errors and optimizing the performance of the ADC. This is crucial in battery-powered devices or applications with strict power constraints. This techniques can be performed while the image sensor

is in operation, allowing for continuous correction of errors. This enhances the overall accuracy and stability of the ADC over time.

Future Scope

The ADC can be integrated into digital cameras, smartphones, and medical imaging devices, with a focus on optimizing performance for specific imaging requirements such as low-light sensitivity and fast frame rates. Research can focus on improving the power efficiency of the ADC through new circuit techniques and optimization for lower power consumption. There is a demand for higher-resolution and faster-readout ADCs. Future research can explore ways to increase resolution and speed while maintaining or improving performance metrics. ADCs can be optimized for AI applications like object recognition and image classification by incorporating features such as on-chip neural network accelerators and advanced data compression techniques. The ADC's performance makes it suitable for automotive and industrial imaging systems. Research can focus on adapting the ADC for applications such as autonomous vehicles and industrial inspection systems, optimizing performance for harsh operating conditions.

References

1. Q. Zhang, N. Ning, J. Li, Q. Yu, Z. Zhang, and K. Wu, ‘‘A high area efficiency 14-bit SAR ADC with hybrid capacitor DAC for array sensors,’’ *IEEE Trans. Circuits Syst. I, Reg. Papers*, early access, Jun. 9, 2020, doi: .1109/TCSI.2020.2998473.

2. R. Xu, B. Liu, and J. Yuan, ‘‘Digitally calibrated 768-kS/s 10-b minimum size SAR ADC array with dithering,’’ *IEEE J. Solid-State Circuits*, vol. 47, no. 9, pp. 2129–2140, Sep. 2012.

3. J.-B. Kim, S.-K. Hong, and O.-K. Kwon, ‘‘A low-power CMOS image sensor with area-efficient 14-bit two-step SA ADCs using pseudomultiple sampling method,’’ *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 62, no. 5, pp. 451–455, May 2015.

4. M.-K. Kim, S.-K. Hong, and O.-K. Kwon, ‘‘A small-area and energy efficient 12-bit SA-ADC with residue sampling and digital calibration for CMOS image sensors,’’ *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 62, no. 10, pp. 932–936, Oct. 2015.

5. M.-W. Seo, S.-H. Suh, T. Iida, T. Takasawa, K. Isobe, T. Watanabe, S. Itoh, K. Yasutomi, and S. Kawahito, ‘‘A low-noise high intrascene dynamic range CMOS image sensor with a 13 to 19b variable-resolution column-parallel folding-Integration/Cyclic ADC,’’ *IEEE J. Solid-State Circuits*, vol. 47, no. 1, pp. 272–283, Jan. 2012.

6. T. Yasue, K. Kitamura, T. Watabe, H. Shimamoto, T. Kosugi, T. Watanabe, S. Aoyama, M. Monoi, Z. Wei, and S. Kawahito, ‘‘A 1.7-in, 33-mpixel, 120-frames/s CMOS image sensor with depletionmode MOS capacitor-based 14-b two-stage cyclic A/D converters,’’ *IEEE Trans. Electron Devices*, vol. 63, no. 1, pp. 153–161, Jan. 2016.

7. K. Nie, W. Zha, X. Shi, J. Li, J. Xu, and J. Ma, ‘‘A single slope ADC with row-wise noise reduction technique for CMOS image sensor,’’ *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 67, no. 9, pp. 2873–2882, Sep. 2020.

8. Y. Shinozuka, K. Shiraishi, M. Furuta, and T. Itakura, ‘‘A single-slope based low-noise ADC with input-signal-dependent multiple sampling scheme for CMOS image sensors,’’ in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2015, pp. 357–360.

9. T. Toyama, K. Mishina, H. Tsuchiya, T. Ichikawa, H. Iwaki, Y. Gendai, H. Murakami, K. Takamiya, H. Shiroshita, Y. Muramatsu, and T. Furusawa, ‘‘A 17.7 Mpixel 120fps CMOS image sensor with 34.8Gb/s readout,’’ in *Proc. IEEE Int. Solid-State Circuits Conf.*, Feb. 2011, pp. 420–422.

10. S. Yoshihara, Y. Nitta, M. Kikuchi, K. Koseki, Y. Ito, Y. Inada, S. Kuramochi, H. Wakabayashi, M. Okano, H. Kuriyama, J. Inutsuka, A. Tajima, T. Nakajima, Y. Kudoh, F. Koga, Y. Kasagi, S. Watanabe, and T. Nomoto, ‘‘A 1/1.8-inch 6.4 MPixel 60 frames/s CMOS image sensor with seamless mode change,’’ *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2998–3006, Dec. 2006.