A 12-BIT COLUMN-PARALLEL TWO-STEP SINGLE SLOPE ADC WITH A FOREGROUND CALIBRATION FOR CMOS IMAGE SENSORS

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Abstract: A unique analog-to-digital converter (ADC) for high-speed CMOS image sensors that is 12-bit column-parallel and two-step single-slope (SS). The small electronic device known as a CMOS image sensor, or complementary metal-oxide-semiconductor image sensor, is essential to the capture of the pictures we see on our digital cameras, cellphones, and other imaging devices. It serves as the "electronic eye" of these gadgets, processing and displaying digital information from light.To reduce non-uniformity in column-level ADCs, a novel correlated double sampling (CDS) method is used in conjunction with the output offset storage (OOS) technology. The comparator's decision point in the suggested structure is independent of the input signal. The input level-induced variation in the comparator offset is removed. The non-idealities from the column ADC and the ramp generator are both corrected via a foreground calibration.

A two-step conversion procedure is used by the ADC. A coarse conversion and a fine conversion are the two stages of the conversion process. Comparing this two-step method to conventional single-slope ADCs enables faster conversion times.

The suggested ADC, designed and simulated on a 130nm CMOS process, achieves +0.76/−0.8 LSB for differential non-linearity and +1.06/−0.84 LSB for integral non-linearity at 100 KS/s sampling frequency with calibration. Also, there is an improvement in the effective number of bits (ENOB) from 4.66 bits to 11.25 bits. With a power consumption of 72 µW, the single ADC has an active area of 7.5 × 775 µm2.

Introduction

Digital single-lens reflex (DSLR) cameras, digital camcorders, and medical equipment all make extensive use of the CMOS Image Sensor (CIS), a crucial component of the visual system.CMOS Image Sensor is a semiconductor device that functions as a "electronic eye". The need for CMOS imagers with high resolution format, fast frame rate, and high ADC resolution has increased significantly with the advancement of digital imager technology.Although the concept for a CMOS (complementary metal oxide semiconductor) image sensor was developed in the second half of the 1960s, the device wasn't put into production until the 1990s when

microfabrication techniques improved to the point where they were practical. The majority of image sensors used in modern digital cameras and smartphones are either CMOS or CCD (charge coupled device) technologies.CMOS and CCD are semiconductor devices that function as "electronic eyes." Despite using photodiodes in common, their production processes and methods for signal reading are different. Because of its higher sensitivity and image quality, CCD technology was initially dominant; but, starting in 2004, CMOS sensors began to outsell CCD sensors in terms of shipping volume.An array of capacitors in a charge-coupled device (CCD) image sensor holds an electric charge that is proportional to the pixel's light intensity. Every capacitor in the array shares its contents with its neighbor via a control circuit, and the last capacitor discharges its charge into a charge amplifier. CCD sensors use a data transport method known as the bucket brigade. A complementary metal oxide semiconductor (CMOS) image sensor, on the other hand, enables the individual amplification of pixel signals by having a photodiode and a CMOS transistor switch for every pixel. The pixel signals may be accessed directly, consecutively, and considerably more quickly than with a CCD sensor by manipulating the matrix of switches. Another benefit of having an amplifier in each pixel is that it reduces noise in the electrical signals that are read after being converted from collected light.Over the last several years, pixel size has decreased steadily, going from the 10–20 micron large pixels that dominated devices in the mid-1990s to the 6–8 micron sensors that are presently overtaking the market. The need for progressively smaller electronic image devices—like phone and security cameras—has led designers to reduce pixel sizes even further. In smaller array devices, image sensors with 4-5 micron pixels are used; however, 3–4 micron pixel sizes are needed for multi-megapixel semiconductors. CMOS image sensors have to be manufactured on 0.25-micron or smaller fabrication lines to reach these dimensions. Narrower line widths allow for the packing of more transistors per pixel element with acceptable fill factors, as long as scaling ratio factors are close to unity. Advanced technologies, including in-pixel analog-to-digital converters, full-color processing, interface logic, and other related sophisticated circuitry designed to enhance the flexibility and dynamic range of CMOS sensors, could become available with 0.13 to 0.25-micron production lines.The process stages for adding color filters and microlens arrays are missing from many CMOS fabrication facilities, but as market needs increase, these processes are being incorporated more often for the manufacturing of image sensors. Furthermore, clean rooms and flat-glass handling equipment are needed for optical packaging processes, which are essential to imaging devices but are often absent from facilities that make ordinary logic and processor integrated circuits. As a result, ramp-up costs for the manufacture of image sensors may be high.

TWO-STEP ADC

The proposed column ADC consists of a multistage comparator, a sampling capacitor (CS), a holding capacitor (CH), a set of switches, delay control logic, and data memory are used to enhance the gain of each amplifier, which are 17 dB, 17dB, and 62dB, respectively. Since the gain of the preAmp1 is only 1, the noise contribution of the PreAmp1 and the PreAmp2 both need to be taken into account. Thanks to the OOS technique(or auto-zeroing), the input-referred noise of the preAmp1 is shaped by a comb filter. The low frequency noise component is suppressed. The simulation shows that the input-referred noises of the preAmp1 and the preAmp2 are 49 μVrms and 36 μVrms, respectively. The simplified schematic of the multistage comparator.

With the simplified schematic shown in Fig. 1(a), the main operation of the proposed column ADC is performed in four phases: reset sampling, signal sampling, coarse A/D conversion, and fine A/D conversion. Reset Sampling. First, with switches RX, SS, SH, SR, and SA close, a reset voltage *Vreset* from the pixel is sampled by CS. Then, when the switch RX is turned off, the error the resistor DAC-based ramp generator, which is shared by all column ADCs, is composed of two parts: a coarse ramp *VRC* for *M*-bit coarse conversion and a fine ramp *VRF* for *N*-bit fine conversion. The total bit (*T*-bit) resolution of the proposed ADC is $T = M + N$. The CS is utilized to sample the reset voltage and the signal voltage, which are both supplied by 4-T APS. The CH is connected in series with the ramp generator. The top plate of the CH is applied to store the final determined charge in the coarse conversion. This charge represents the coarse conversion residue. Moreover, the bottom plate of the CH is driven by the fine ramp to realize the fine conversion. Through the delay control logic, the decision error that occurs in the coarse conversion can be relaxed. The conversion results are latched by the column memory. *VCM*1 and *VCM*2 are the common-mode voltages of the PreAmp1 and the PreAmp2, where *VCM*1 = 1.6 V and *VCM*2 = 0.8 V. To remove the pixel offsets, a multistage comparator topology with output offset storage (OOS) [22] technique has been used to conduct the CDS operation. Due to the single-ended structure, the input swing of the preAmp1 needs to cover the range of the analog input signal for correct conversion. Hence, in the preAmp1, the PMOS transistors are used for input pairs and the supply voltage is 3.3 V.

To prevent the output of the preAmp1 from being saturated, the gain of the preAmp1 is set to 1. Thanks to the direct-current (DC) split of the offset storage capacitor CD, other pre-amplifiers can be designed with 1.2V supplies to reduce the power consumption. From the preAmp2 to preAmp4, the NMOS input pairs voltage *VE* from RX, which includes the charge injection and the clock feed through, is also sampled by CS after a certain time delay. Next, by sequentially turning off SR and SS, the signal-dependent switch errors caused by the sampling switch SS are both eliminated. Finally, through the coarse ramp switch SC, the maximum voltage *VCT* of the coarse ramp is loaded into the left plate of the CS (or voltage node P2). The resulting positive input voltage of the comparator *VP*1 is,

$$VP1 = VCM1 - (Vreset + VE - VCT)$$

where *VS* is the actual signal that corresponds to the incident light intensity. Then, SC is open and SR, SS are closed. The signal voltage *Vsignal* is sampled by CS. Next, similar to the reset sampling phase, the SR is turned off before the SS. Coarse A/D conversion. With the closure of the SC, the left plate of the CS is driven by the coarse ramp *VRC*. Considering the stored charge on the CD, the equivalent voltage at the input node P1 is calculated from ,

$$V'P1 = VCM1 + (VS - (VCT - VRC)).$$

The input offset of the preAmp1, the reset signal from the pixel, and the charge errors from the RX are all canceled. Hence, with the output coupling capacitor CD, the CDS operation based OOS is realized. The essence of the conversion is to determine the sign of $V'P1 - VCM1$. During the coarse A/D conversion, *VRC* starts in synchrony with the coarse counter and sweeps from *VCT* to $VCT - VFS$, where *VFS* is the fullscale voltage. If the signal *VS* is,

$$VCM1 + (VS - (m + 1)\ (VRC)') < VCM1 < VCM1 + (VS - m\ V'RC),$$

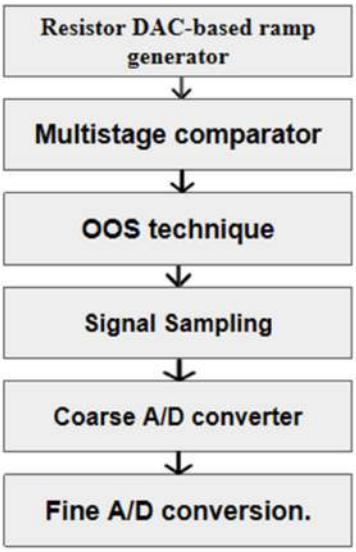


Fig.2.1 Block Diagram of the proposed Two Step SS ADC

The input offset of the preAmp1, the reset signal from the pixel, and the charge errors from the RX are all canceled. Hence, with the output coupling capacitor CD, the CDS operation based OOS is realized. The essence of the conversion is to determine the sign of $V'P1 - VCM1$. During the coarse A/D conversion, VRC starts in synchrony with the coarse counter and sweeps from VCT to $VCT - VFS$, where VFS is the fullscale voltage. If the signal VS is,

$$VCM1 + (VS - (m + 1)\ (VRC)') < VCM1 < VCM1 + (VS - m\ V'RC),$$

The comparator output VO will be changed to the logic low when $VCT - VRC$ becomes (m + 1) $V'RC$. $V'RC$ is the minimum conversion voltage of the coarse ramp, which is $VFS / 2M$. Then, the upper M-bit memory stores the coarse counter value as the coarse A/D result DM and SH is turned off. At this moment, the bottom plate charge of the CH (node P3) is,

$$QCH = Vref - (VCT - (m + 1)\ V'RC) \times CD$$

When VRC drops to $VCT - VFS$, the coarse conversion is over and the SC is open. Fine A/D conversion. When SF is closed, the fine ramp signal VRF is coupled to the positive input of the comparator through the CH. According to the charge conservation, the equivalent voltage at the input node P1 is obtained from ,

$$V'P1 = VCM1 + (VS - (m + 1)\, C') + VRF - Vref$$

where $VRF - Vref$ is the effective fine ramp voltage. Since the fine ramp signal VRF spans from $Vref + V'RC$ to $Vref$, the variation of the resulting coupling voltage $V'P1$ is $V'RC$, as illustrated in the gray line of Figure. The step of the fine ramp is $V'RF$, which is $V'RC/2N$. When $V'P1$ drops below the $VCM1$, the comparator output VO is changed to the logic low again and the lower N-bit memory stores the fine counter value as the fine A/D result DN. Therefore, the final digital output $DOUT$ is calculated from:

$$DOUT = 2\,N \times DM + DN - 2\,N$$

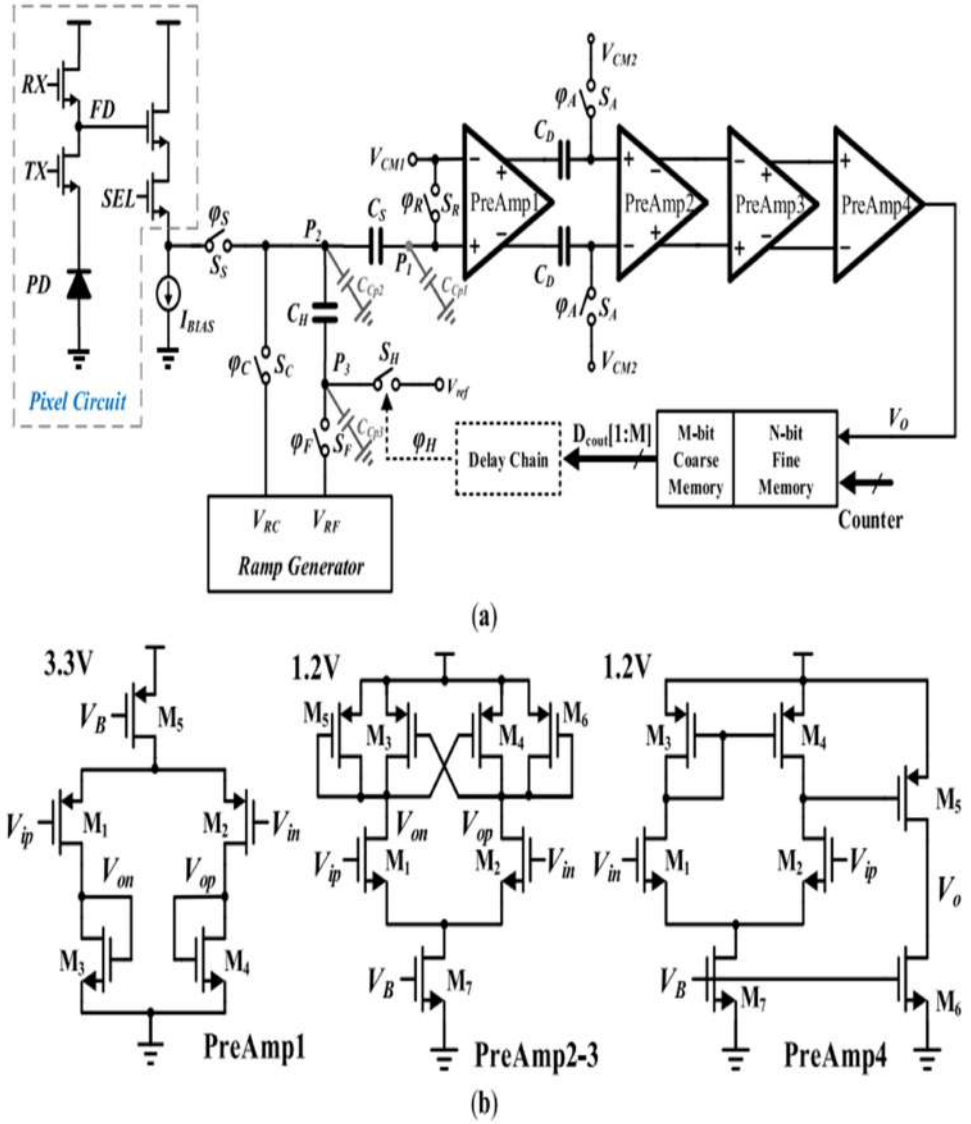


Figure.2.2 Simplified schematics of (a) the proposed two-step SS ADC with the 4 T-APS and (b) the multistage comparator

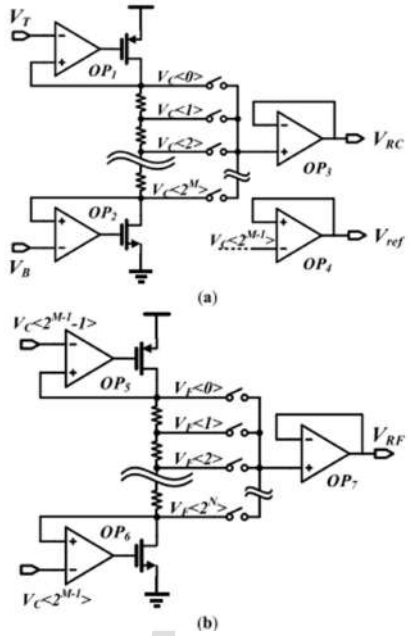
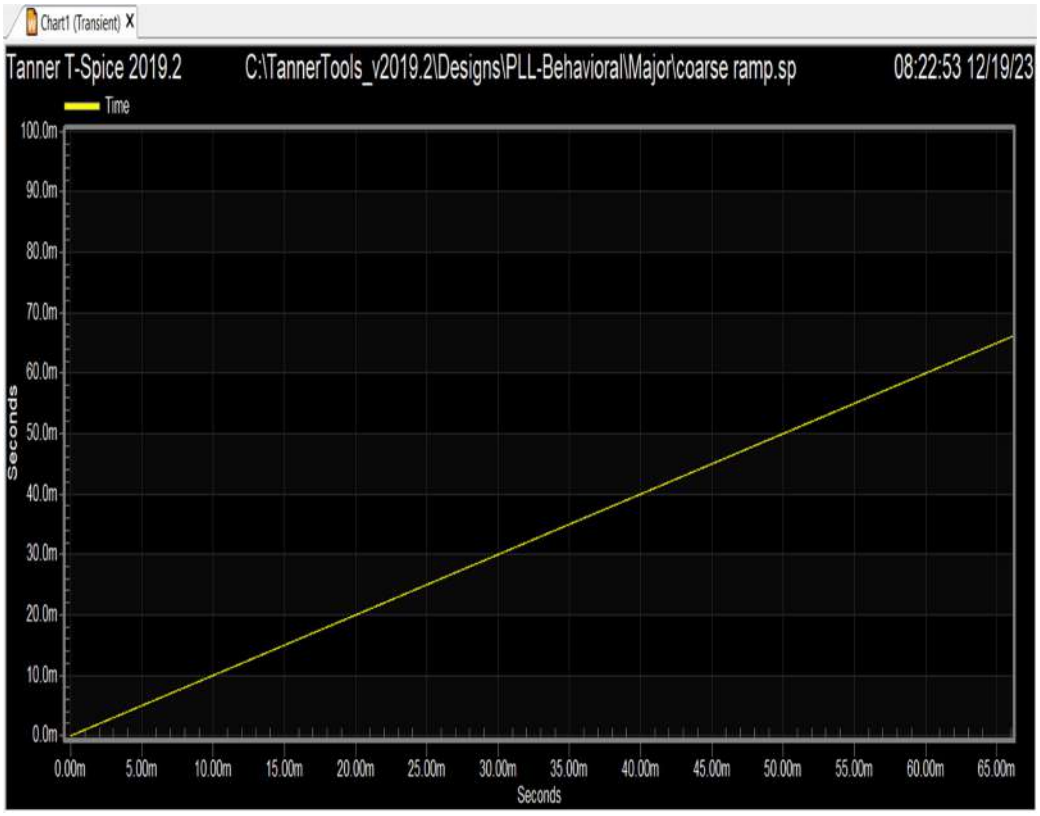


Figure 2.3: Simplified schematics of the ramp generator. (a) Coarse Ramp (b) Fine Ramp

Result and it's discussion

The primary result of the ADC is the digital representation of the converted analog signal of the fine and coarse ramp generator output.



(a) (b)

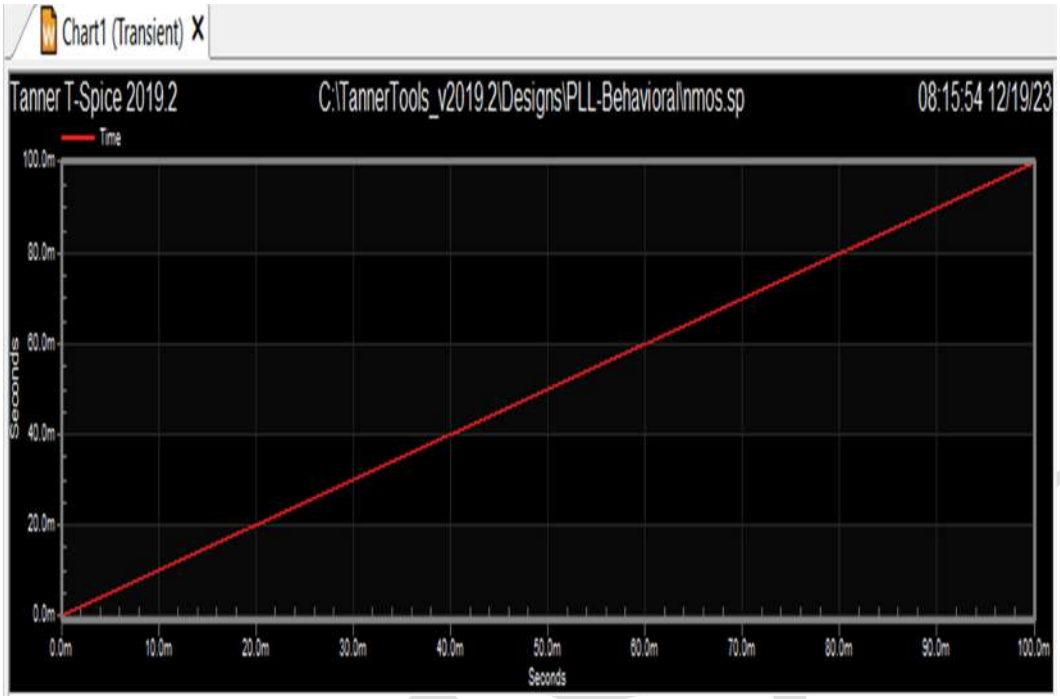


Figure 7.1: (a) Timing diagram of the coarse conversion ramp (b) Timing diagram of the fine conversion ramp

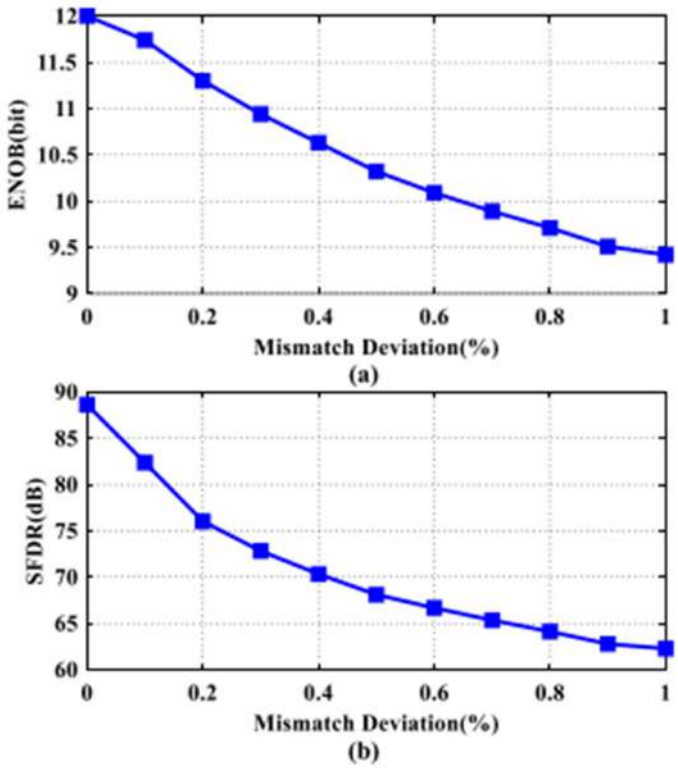


Figure 7.2: The dynamic performance versus mismatch deviation.
(a) ENOB; (b) SFDR

To investigate the effect of resistor mismatch on the ADC performance, Fig. 7.2 shows the simulated averaged ENOB and SFDR as a function of mismatch deviation $\sigma(1$ R/R). As can be seen, the linearity of the column ADC is deteriorated severely as the resistor mismatch increases. When the mismatch deviation remains at 1%, the ENOB and SFDR are only 9.42 bits and 62.27 dB, respectively.

CONCLUSION AND FUTURE SCOPE

Conclusions

A novel 12-bit column-parallel two-step single-slope (SS) analog-to-digital converter (ADC) for high-speed CMOS image sensors. Cooperating with the output offset storage (OOS) technique, a new correlated double sampling (CDS) is adopted to reduce the non-uniformity in column-level ADCs. In the proposed structure, the decision point of the comparator is independent of the input signal. The variation of the comparator offset caused by the input level is eliminated.DNL) of +0.76/−0.8 LSB
and the integral nonlinearity (INL) of +1.06/−0.84 LSB at a sampling frequency of 100 KS/s with the calibration. The effective number of bits (ENOB) is also improved from 4.66 bits to 11.25 bits. The single ADC occupies an active area of 7.5 × 775 μm2 and the power consumption is 72 μW.

Future Scope

In the column ADC, non-idealities such as charge errors of MOS switches, parasitic capacitors, and comparator offsets can also make the proposed structure malfunctioned. Similarly, to calibrate the slope degradation of the coarse ramp caused by parasitic capacitors, the range of the original coarse ramp is also slightly extended analyzed.Through a foreground calibration, the non-idealities from the ramp generator and the column ADC are both corrected and also to minimizing power consumption by continuously correcting errors and optimizing the performance of the ADC. This is crucial in battery-powered devices or applications with strict power constraints. This techniques can be performed while the image sensor is in operation, allowing for continuous correction of errors. This enhances the overall accuracy and stability of the ADC over time.The use of a foreground calibration approach allows for adaptability to changes in environmental conditions or aging effects, ensuring the long-term reliability and stability of the ADC.

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