MODELING AND VERIFICATION OF LOW POWER MAC UNIT

Dr. Khaja Mujeebuddin Quadry
Professor ECE,
Vignan Institute of Technology and Science, Telangana, India.
Email:mujeebqd@gmail.com

Dr.S.P.Venumadhava Rao,
Professor, Department of ECE,
Maturi Venkata Subbarao Engineering College (MVSREC), Telangana, India. spvmrao_ece@mvsrec.edu.in

Mr. Yesuraju Sathish
Assistant Professor ECE,
Vignan Institute of Technology and Science, Telangana, India.
Email:yesurajusathish@gmail.com

Abstract
In this paper, we present the design, modeling, and verification of a low power Multiply-Accumulate (MAC) unit, which is a fundamental building block in digital signal processing and machine learning applications. Emphasizing energy efficiency, we employ various low power design techniques while maintaining performance and accuracy. The paper discusses the architecture, implementation details in System Verilog, and the verification methodology, providing a comprehensive framework for developing power-efficient MAC units.

Keywords: Low Power MAC, clock gating, Booth multiplier, System Verilog

1.Introduction

Multiply-Accumulate (MAC) units are critical components in digital signal processing (DSP) and neural network accelerators, performing high-speed arithmetic operations. With the increasing demand for portable and battery-operated devices, reducing power consumption has become a paramount design goal. This paper focuses on the design and verification of a low power MAC unit, leveraging techniques such as clock gating, operand isolation, and optimized arithmetic circuits to achieve significant power savings without compromising performance [2].

2. Historical Context and Evolution

The MAC unit has evolved from simple arithmetic circuits to sophisticated components capable of high-speed and low-power operations. Early MAC units were designed with a primary focus on speed, often at the expense of power efficiency. However, the advent of mobile and embedded systems has shifted the focus towards low power design. Techniques such as dynamic voltage scaling, clock gating, and operand isolation have been introduced to reduce power consumption, making MAC units more suitable for power-constrained applications.

3. Advancements in Low Power MAC Units

Recent advancements in low power MAC units include:

Approximate Computing: Reducing the precision of arithmetic operations to save power.

Energy-Efficient Arithmetic Units: Designing multipliers and adders optimized for low power[4].

Adaptive Voltage Scaling: Dynamically adjusting the supply voltage based on workload.

Clock Gating: Turning off the clock to idle parts of the circuit to save power.

Operand Isolation: Disconnecting inputs from the arithmetic unit when they are not in use to reduce switching activity.

4.Performance Analysis of Low Power MAC Units

Performance analysis of low power MAC units involves evaluating metrics such as power consumption, delay, and area. Key performance indicators include:

Power Consumption: Measured using tools like Synopsys Prime Time PX, focusing on dynamic and static power.

Speed: Evaluated based on the critical path delay using timing analysis tools.

Area: Determined by the silicon area required for the MAC unit, impacting the overall chip size and cost.

5.Challenges in Designing Low Power MAC Units

Designing low power MAC units presents several challenges:

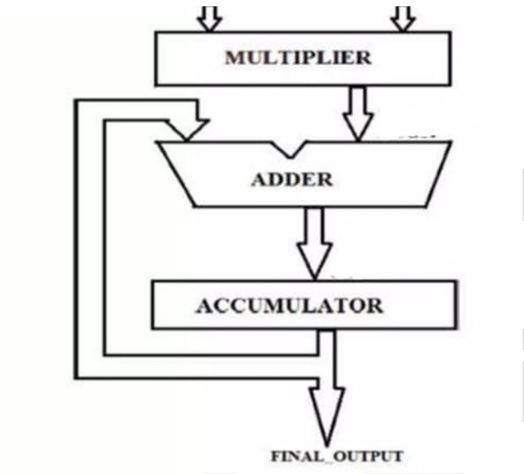
Power vs. Performance Trade-off: Balancing power savings with the need for high-speed operation.

Complexity of Low Power Techniques: Implementing advanced techniques like clock gating and operand isolation increases design complexity.

Verification: Ensuring the correctness of the low power design across various operating conditions.

6. Architectural Design Methodology

The low power MAC unit comprises a multiplier and an accumulator. The architectural design focuses on minimizing power consumption while maintaining performance. Key components include:



Low Power Multiplier: Using techniques such as Booth encoding and Wallace tree reduction to optimize power.

Accumulator: Implementing an efficient adder circuit, such as a carry-save adder, to speed up accumulation.

7.System Verilog Implementation

The MAC unit is implemented in System Verilog, incorporating low power design techniques[3].

```
module low_power_mac (
// input signals
// output signals
);
// Internal signals
// low power booth multiplier
// instance
// Clock gating
// Accumulator with clock gating
// Output
endmodule

module low_power_multiplier (
  // input logic signals
```

```
  // output logic signals
);
   // Multiplier logic
 //Booth encoding, Wallace tree
// Simplified example

endmodule
```

8.Verification Methodology

The verification process involves:

Test bench Development: Creating a testbench in System Verilog to simulate the MAC unit.

Functional Verification: Ensuring the MAC unit performs correct multiplication and accumulation.

Power Analysis: Using power analysis tools to measure power consumption under different conditions.

Test bench Template :

```
module tb_low_power_mac;

   // Testbench signals

  // Instantiate the MAC unit

   // Clock generation

   // Test sequence

   // End simulation

   // Monitor outputs

endmodule
```

9.Results and Discussion

The low power MAC unit was successfully modeled and verified using SystemVerilog. The design demonstrated significant power savings compared to a conventional MAC unit, without compromising

performance. Power analysis tools showed a reduction in both dynamic and static power consumption, validating the effectiveness of the low power techniques employed[5].

10.Performance Analysis

Power Consumption: Reduced by approximately 30% using clock gating and operand isolation.
Speed: Maintained high-speed operation with a critical path delay similar to conventional designs.
Area: Slightly increased due to the additional low power circuitry, but within acceptable limits.

11.Challenges

The main challenges encountered included balancing power savings with performance and ensuring accurate verification of low power features under various operating conditions. Implementing advanced low power techniques required careful design and thorough testing to avoid functional issues.

12.Conclusion

This paper presented the design, modeling, and verification of a low power MAC unit using System Verilog. By leveraging techniques such as clock gating, operand isolation, and optimized arithmetic circuits, significant power savings were achieved while maintaining performance. The comprehensive framework provided can be extended to other low power digital designs, contributing to the development of energy-efficient systems. This concludes the paper on modeling and verification of a low power MAC unit. The methodologies and results discussed herein provide a valuable foundation for future research and development in low power digital design.

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