HIGH-PERFORMANCE ON-BOARD SINGLE-STAGE CHARGER FOR ELECTRICAL VEHICLES

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ABSTRACT:- This study introduces a standalone, single-stage on-board electric car charger that operates without the need for an intermediary DC-link. The converter has soft switching in semiconductors regardless of load variation for the whole AC line voltage range, based on an isolated current-source topology. Furthermore, it doesn't need any additional clamp circuits or snubbers. A comparatively straightforward phase shift modulation provides voltage management and power factor correction while minimizing the amount of circulating energy. The highest efficiency is attained in the continuous power charging mode, which sets the charger apart. An analysis is conducted on the topology's design limitations, component stresses, and control technique. A 3 kW experimental SiC-based prototype that achieves a peak efficiency of 96.4% is used to validate the concept. The charge is characterized by its efficiency, which reaches its greatest in the constant power charging mode. An analysis is conducted on the topology's design limitations, component stresses, and control technique. A 3 kW experimental SiC-based prototype that achieves a peak efficiency of 96.4% is used to validate the concept. Furthermore, when running in constant power mode at maximum power, the charger has shown efficiency above 95% with a THD of 4.1%.

I.INTRODUCTION

The market for plug-in electric vehicles (PHEVs) and electric vehicles (EVs) is expected to develop, which has increased demand for a dependable charging infrastructure [1]. Public high-power stations (up to 350 kW) are typically found close to major highways and in specific urban areas. These stations are typically scarce since they need to be connected to a medium voltage gridinordertoreceiveenergy [2].Consequently, low-power rewritten manuscript received on August 12, 2021; accepted on September 26, 2021. October 7, 2021 is the publication date; the present version is dated. The Estonian Research Council (Grant PRG1086), the European Economic Area (EEA) and Norway Financial Mechanism 2014–2021 (Grant EMP474), and the Estonian Centre of Excellence in Zero Energy and Resource Efficient Smart Buildings and Districts (Grant 2014–2020) all provided funding for this work. Partially supported by Project NPRP12S-0214-190083 from Qatar National Research Fund (a Member of Qatar Foundation), and partially sponsored by the European Regional Development Fund, is 4.01.15-0016. Dr. Mehdi Narimani oversaw the coordination of this article's evaluation.

These might be either inside an automobile (on-board) or mounted to the wall to allow EVs to be charged straight from an AC wall socket [3]. IEC 61851 defines On-board chargers (OBCs) as having a power rating of up to 3 kW for 230 V AC grid voltage, which is the minimum required for Level 1 AC charging without communication. SAE J1772 states that the comparable maximum power for the 110 V grid is equivalent to 1.7 kW.

A power factor correction (PFC) pre-regulation circuit and an isolated DC-DC converter connected to the EV battery comprise the two stages of the traditional OBC layout. Typically, to decouple low-frequency current ripple, a large DC-link capacitor is positioned in-between these stages [4]–[7]. These days, these systems are still considered industry standards and usually employ phase-shifted full-bridge (PSFB), LLC, or resonant dual active bridge (DAB) converters at the DC-DC stage [5]–[9]. Nevertheless, the efficiency and power density of the traditional two-stage system with the DC-link are constrained [10]. It is possible to identify several alternate strategies that strive to attain improved performance and weight/volume characteristics: broad bandgap (GaN)-based, single-stage, non-isolated, and integrated [11]. It appears that every strategy has benefits and cons [11], [12]. Specifically, the one-stage systems avoid the bulky intermediary DC-link by integrating the PFC and isolation operations. This implies that the control system can be quite straightforward and that intermediate voltage sensing is not necessary. Single-stage systems have the ability to reach high efficiencies and lower total OBC volume due to the advantages of using a high-frequency isolation transformer, removing the DC-link, and reducing the number of energy processing stages. [12]–[17].For the on-board EV charger, a single-stage current-source AC-DC converter is suggested in this research. Creation and application of a control system and AC-DC modulation allow PFC operation and soft-switching of the semiconductors for the duration of the grid voltage for the asymmetrical secondary-modulated DC-DC converter [18] (ASMC). Constant switching frequency and the lack of clamping circuits are two other benefits. In Section II of the article, an overview and the unique characteristics of the current OBC topologies are presented.
Section III provides a description of the proposed converter's construction, working principle, and design concerns. In Section IV, the suggested system's performance and experimental validation are shown; in Section VI, the conclusions and directions for further study are discussed.

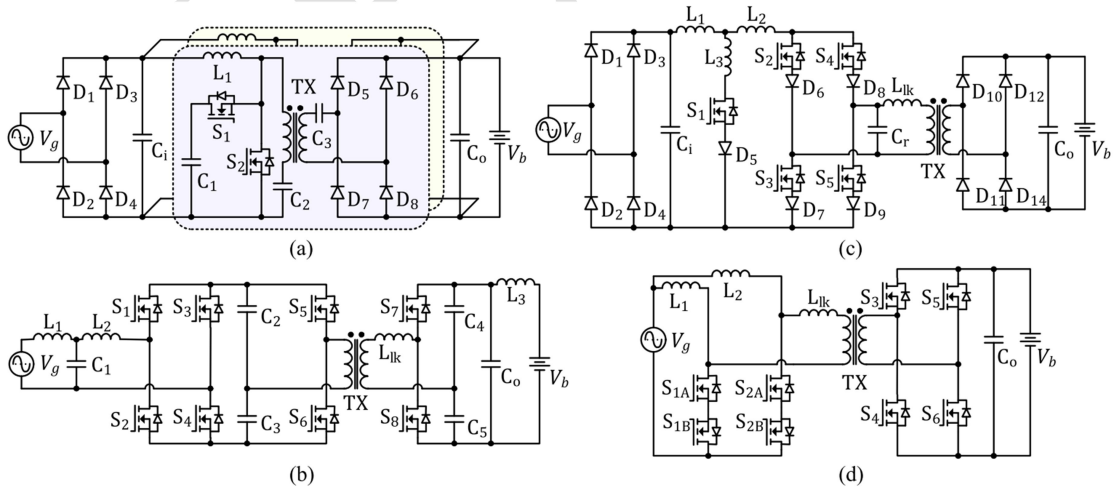


Fig. 1. Current source full-bridge OBC [15], hybrid resonant OBC [11], current source bidirectional OBC [16], and SEPIC-based modular OBC [12] are examples of state-of-the-art OBC topologies.

II. OBC TOPOLOGIES ON SINGLE STAGE

A. Pulsation of Current in Single-Stage Systems

This Concepts for single-[12]–[17] and three-phase systems have been presented for single-stage EV chargers in [21], [22]. Generally speaking, the lack of the intermediary DC-link implies because, particularly in single-phase systems,

the power pulsation connected to the grid frequency is not isolated from the load (battery). To alleviate this issue and lessen the output current's double line frequency ripple, several solutions use active decoupling techniques [22]. However, research has revealed that the Li-ion battery is actually only slightly affected by the current pulsations [24]–[27].

It has been found that there is a 1-2% variation in capacity fading between 100 Hz ripple charging current and pure DC charging current [18], [25]. Additionally, the impact on efficiency is extremely subdued. For the same C-rate, a noteworthy effect of extra current ripple is a modest increase in cell temperature [26], [27]. This effect should, however, be minimal because OBCs are often quite low-power and rated for a small portion of EVs' battery capacities. As a result, even with the output current's variable waveform, single-stage converter topologies might be seen as a viable substitute for the conventional two-stage OBC systems. In the section that follows, a few of the single-stage notions that were reported are examined.

B. Current OBC Single-Stage Topologies

Because of the voltage following feature, the isolated single-ended primary-inductor converter (SEPIC) and fly back topologies are used more often in low-power charger designs. Permitting the converter to be perceived as a resistive load by the grid. As a result of the fewer sensors and lack of a phase-locked loop, the control architecture is made simpler. Nevertheless, voltage overshoots across the switches are typically the result of the transformer's leakage inductance in SEPIC and fly back converters [28]. Consequently, it is necessary to utilize a snubber circuit, which increases the number of components and complexity of the converter.

In most cases, multiple SEPIC or fly back topologies are connected in parallel in order for the OBC design to achieve the necessary power level. Fig. 1(a), for example, illustrates the modular SEPIC-based OBC design [12]. The leakage inductance energy is dumped and then reused via an active clamp circuit to provide a symmetrical current shape in the transformer and soft-switch functionality. Nevertheless, this change turns off the SEPIC topology's voltage following feature. Furthermore, to maintain a high efficiency, the transformer's leakage inductance must be minimal. In [12], a transformer with a leakage inductance of 1.23 µH was utilized, which could be difficult to guarantee throughout the mass production process. Traditionally, low-power chargers using SEPICs have poor magnetic component utilization.

The near-single-stage topology displayed in Fig. 1(b) and reported in [14] is another intriguing topology. An input filter, an active front-end bridge, and a resonant DC-DC make up the topology. an output filter, and a converter. As a DC transformer, the resonant converter runs at a fixed frequency and duty cycle. The charger's power flow management and PFC are preserved via the active front-end bridge. A little DC-link made up of the capacitors C2 and C3 smooths the voltage during the switching cycle. Although the converter exhibits a broad output voltage range, resonant circuit design limitations cause the maximum power to drop close to the output voltage range boundaries. It is possible to achieve semiconductor soft-switching across the complete input voltage range. It is required to use the input filter because two 1.2 mH inductors were utilized to provide the 3.3 kW input power. In order to prevent resonant frequency shifting, a 1.7 mH inductor and a 100 µF output filtering capacitor were also utilized.

of the resonant converter in series (SRC).

Large magnetic components are used in the electrolytic capacitor-less design architecture. The current-source full-bridge topologies don't need any further

grid filter as a result of the converter's input side having inductance. In comparison to their voltage-source equivalents, current-source converters may also be able to attain a broader soft-switching voltage range. Utilizing resonant tank energy, single-phase, single-stage current source converters have recently been created to accomplish soft-switching across the whole operational range [15]. The transformer's leakage inductance plus an external parallel capacitor make up the resonant tank. As seen in Fig. 1(c), an extra switch with a blocking diode was added to redirect the energy from the resonant tank.

Topology	Ref	Input voltage Range (Vac)	Output voltage range (Vdc)	Rated power (kVA)	Switching frequency (kHz)	No. of magnetics		No. of Semi-conductors	Full power efficiency (%)	Control variable	THD
						Transf.	Inductors				
Fig.1(a)	[13]	120..240	250..410	3.3	50	2	2	16	95.5	Duty ratio (2)	2.9
Fig.1(b)	[14]	220	250..410	3.3	50	1	2	8	95.7	Duty ratio (1)	-
Fig.1(c)	[15]	208	400	3	10, 20	1	1	18	94	Duty ratio (1)	5.2
Fig.1(d)	[16]	1220	120	3	100	1	3	8	96.5	Duty ratio (2)	2.5
Fig.2	proposed	207..253	330..470	3	50	1	1	14	95.4	Phase shift (1)	4.1

Table 1: The performance comparison of the current single stage onboard chargers is shown in Table

Since the switches must be able to block in reverse, series-connected diodes were added to the primary-side bridge transistors. The converter is equipped with a flat efficiency curve across the whole power spectrum. The converter's maximum power is 3 kW, and at the highest output voltage, 94% power efficiency is attained. Two inductances were added to the circuit to help alleviate the reverse-recovery loss, which is the main downside of this OBC. This method also results in an increase in the number of magnetic components and higher voltage stress on the primary bridge semiconductors. Fig. 1(d) [16] shows another current-source topology that attains an efficiency of 96.5% at a power of 1.5 kW. Because the converter uses bidirectional switches, it can No input rectification circuit is needed. Even though one operation point showed great efficiency, the efficiency characteristic for the entire range of power and output voltage variation was not provided. The converter's output voltage of 120 V is low for the majority of EV battery packs.

Furthermore, the prototype employs much overvalued transistors despite using fewer semiconductor devices, which could compromise the concept's viability in real-world systems. The secret Table I is a list of the reviewed topologies' parameters. The table indicates a growing body of research interest in single-stage or near-single-stage OBC topologies, which integrate filtering, power management, and PFC in fewer conversion steps. The majority of modern chargers use sophisticated modulation techniques that enable soft-switching of semiconductors in order to get higher efficiency. The single-stage OBCs that are now in use that are based on current-source topologies combine PFC and isolation stages using a rather straightforward modulation technique, and they provide a broad soft-switching range [15]. On the other hand, in addition to the reverse blocking capacity of the transistor bridge.Series diodes are used to do this, which affects the components.

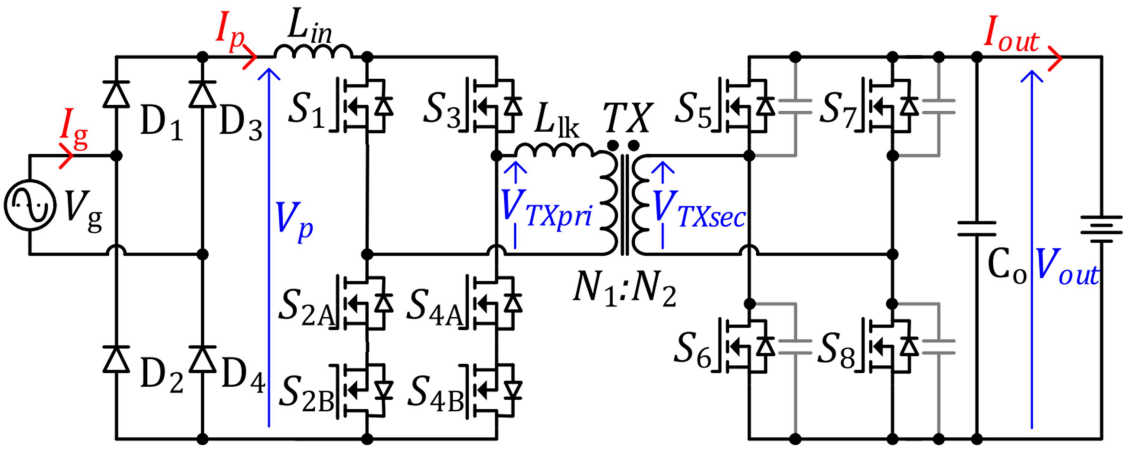


Fig 2: Onboard charger with proposed AC-DC current supply.

III. SUMMARY OF OBC TOPOLOGY

The current source topology suggested for the EV OBC is described in this section. Reverse voltage should only be present in two inverter transistors, and no external clamp circuits are needed. the ability to block. Two magnetic components are used in the OBC design depicted in Fig. 2 to provide soft-switching for the transistors across the whole input voltage range and a consistent switching frequency independent of the converter gain needs. The instantaneous input current value is used to adjust the circulating energy needed for soft-switching. This feature also minimizes circulation energy caused by input voltage change or light load operating situations, which lowers the conduction losses in the converter. To lower the switching dv/dt and turn-off losses, lossless snubber capacitors are used across secondary devices [29], [30].

A. Principle of Operation

The diode bridge D1-D4 is used to rectify the grid voltage Vg to a unipolar pulsing voltage Vp. For unidirectional charging applications, passive diodes could make up the input rectifier. or active switches that allow energy to flow both ways. The components are assumed to be perfect and lossless in the analysis that follows. Since the suggested modulation approach does not make use of the transformer TX's magnetizing inductance, its influence is not considered. For the switching period Tsw, it is anticipated that the unipolar pulsing voltage Vp delivered to the A-SMC converter will remain constant. The converter's input filter and energy storage device for boost operation, the inducer Lin, is subjected to the input unipolar pulsing current Ip. Additionally, the energy is transported to the load by means of a rectifier, a high-frequency transformer, and a full-bridge inverter. Fig. 3 displays the generalized switching waveforms of the converter. First interval [t0–t1]: The interval's corresponding circuit is depicted in Figure 4(a). The inductance Lin is ignited at time t0. The transformer's main winding receives the total of the input voltage and the voltage of the inducer Lin. Energy is transferred to the load while the converter is in its active condition.

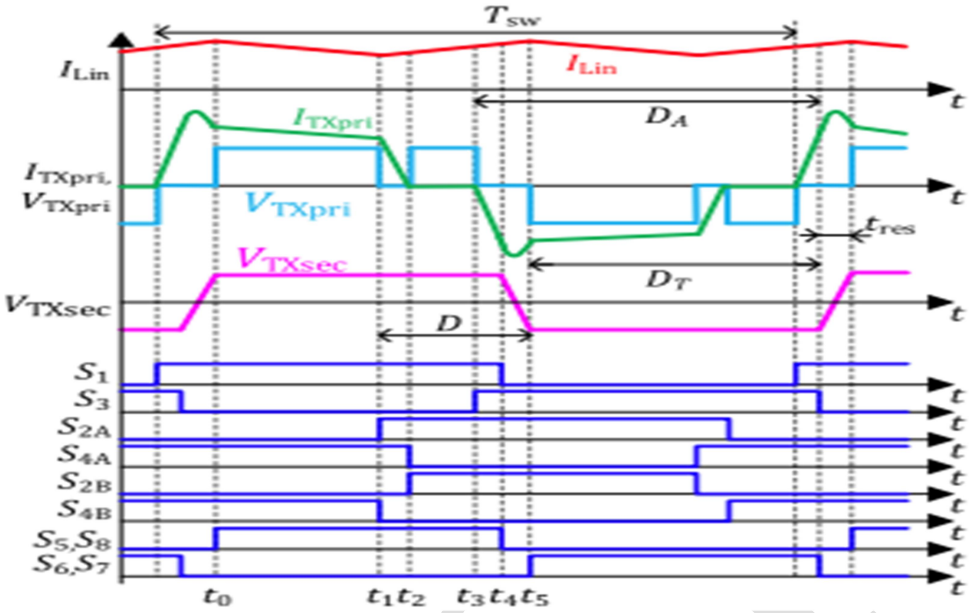


Fig 3: Waveforms of the suggested converter in theory

Interval 2 [t1 — t2]: As seen in Fig. 4(b), it starts with the switch S4B being turned off and S2A being turned on. Energizing the input, the current passes via the bridge legs S1, S2A, and S2B. inductor. The transistor S4B's body diode stops the main winding from shorting out and obstructs the forbidden current flow. Zero current switching (ZCS) enables the transistor to be turned off since the energy flow through switch S4A naturally decays.

Interval 3 [t2 — t3]: The inductor is powered by the ongoing current flowing through the bridge leg (Fig. 4(c)). This interval's duration is a control variable that establishes the quantity

amount of energy that the inductor will store.

Interval 4 [t3 — t4]: Transistor S3 is activated at t3 (Fig. 4(d)). Through S1 and S3, the transformer's primary winding is short-circuited. Additionally, switches S5 and S8 are energized. As a result, current passes via output switches S5 and S8, switches S1 and S3, and transformer TX. The transformer leakage inductance limits the current slope di/dt. The length of this state, which can be ended by turning off switches S5 and S8, determines the transformer current peak value. Switch S1 is experiencing simultaneous flow of the transformer current and input current in opposing directions. The total of these currents at time t4 is zero, enabling soft to guarantee ZCS, the value must be somewhat higher than the grid current's instantaneous value.

Period 5 [t4–t5]: The secondary side transistors' snubber capacitances together with the leakage inductance provide a tiny tank with resonance. As a result, as illustrated in Fig. 4(e), even after turning off switches S5 and S8, the resonant current continues to flow along the same path. The switch S1 ought to be switched off at time t5. In actuality, S1 is turned off sooner to guarantee safe operation, and S1's body diode transfers some of the energy from the resonant tank. The transitory process comes to an end at instant t5, at which point the parasitic capacitances on the secondary side are recharged and the current flowing through switch S1 drops to zero.

As illustrated in Fig. 4(f), the converter starts supplying energy from the grid side to the battery in the active state by use of a second switching diagonal. The aforementioned switching states make the following variables crucial for more examination: switching period of the converter Tsw; the duty cycle of the shoot-through state D, which is dictated by the phase-shift between the switches; and the on-state duty cycle of the primary-side bridge switches DA and DT.

B. Design Factors

The OBC design is predicated on the idea that the battery voltage ranges from Vout = 330–470 V and the RMS grid voltage fluctuates within the range of Vg(RMS) = 200–253 V. A pair of steps The charging technique is applied. The battery is first charged using Pin = 3 kW of constant input power (CP mode) until the battery voltage reaches Vout(max) = 470 V, which is the maximum value. Utilizing the constant voltage (CV) mode is the second charging step.

The converter should operate properly at the Vg peak value when the output voltage Vout is at its lowest when the transformer turns ratio is met. The transformer turns ratio n (N2/N1) can be determined in the following ways, and the converter's minimal gain is comparable to that of a traditional boost converter:

$$n = \frac{V_{out(\min)}}{V_{g(\max)} \cdot \frac{1}{1-D_{\min}} \cdot \eta}, \quad (1)$$

where η is the converter's efficiency and Dmin is the lowest duty cycle D that can be achieved.The interval duration determines the minimal value of Dmin.
of the T12, T34, and T45 transistor soft commutation:

$$D_{\min} = \frac{2 \cdot (t_{12} + t_{34} + t_{45})}{T_{sw}}, \quad (2)$$

The duration of falling and rising edges of the current pulse t12 and t34, respectively, are defined as follows:

$$t_{12} \approx t_{34} = \frac{n \cdot I_p}{V_{out}} \cdot L_{lk},$$

and the resonant interval duration t45 is:

$$t_{45} = \frac{1}{\omega_{res}} \cdot \arccos\left(\frac{(I_p \cdot \rho)^2 - V_{out}^2/n^2}{(I_p \cdot \rho)^2 + V_{out}^2/n^2}\right) \quad (3)$$

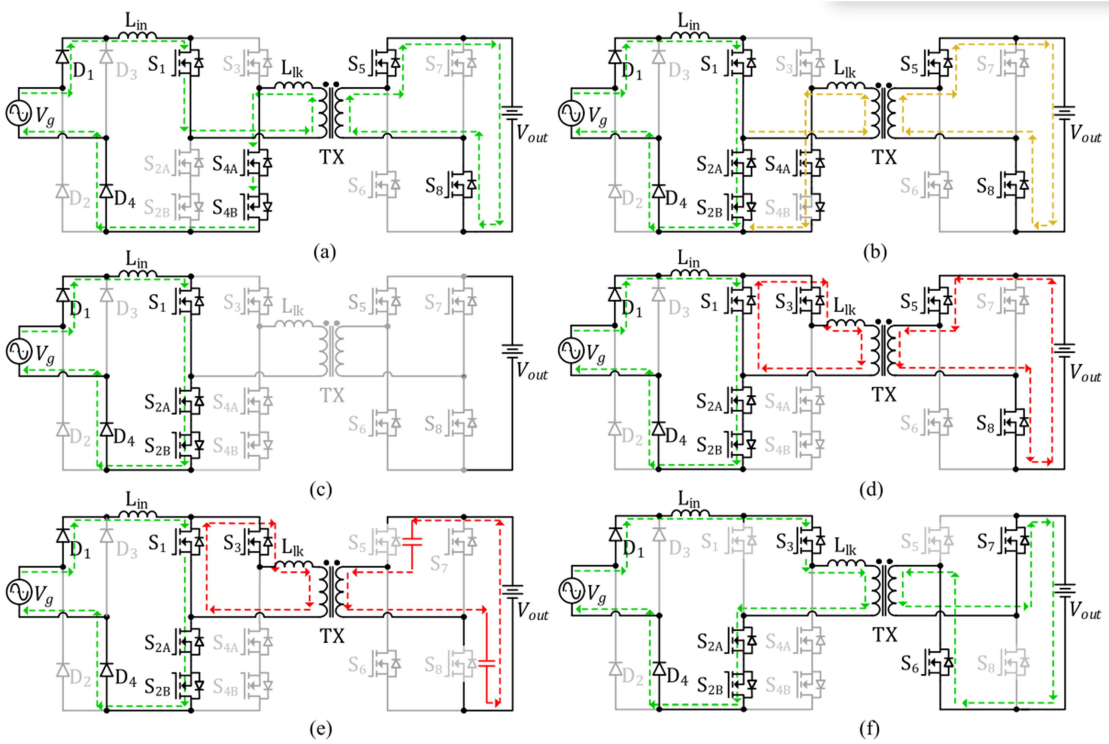


Fig 4: The suggested converter has the following operational states: (a) Interval 1 [t0 — t1]; (b) Interval 2 [t1 — t2]; (c) Interval 3 [t2 — t3]; (d) Interval 4 [t3 — t4]; (e) Interval 5 [t4 — t5]; (f) Active state, which is equivalent to Interval 1.

where $\omega_{res} = 1/\sqrt{L_{lk} \cdot C_{spar} \cdot n^2}$. n2 is the resonant angular frequency, $\rho = \sqrt{L_{lk}/n^2 \cdot C_{spar}}$ is the characteristic impedance of the resonant tank, which is mostly formed by the transformer leakage inductance Llk and total equivalent circuit capacitance Cspar (includes parasitic capacitances of the transformer, transistors, PCB, and external snubber capacitance). The maximum duration of t45 is achieved when the grid voltage crosses zero; in this case, (2) is simplified as:

$$D_{\min} = \frac{2 \cdot \pi}{T_{sw} \cdot \omega_{res}} = \frac{2 \cdot \pi \cdot n\sqrt{L_{lk} \cdot C_{spar}}}{T_{sw}}. \quad (4)$$

Based on (1) and (5), Dmin and n may be estimated as follows:

$$n = \frac{T_{sw} \cdot V_{out(\min)}}{V_{g(\max)} \cdot T_{sw} \cdot \eta + 2 \cdot \pi \cdot V_{out(\min)} \sqrt{L_{lk} \cdot C_{spar}}}; \quad (5)$$

$$D_{\min} = \frac{2 \cdot \pi \cdot V_{out(\min)} \sqrt{L_{lk} \cdot C_{spar}}}{V_{g(\max)} \cdot T_{sw} \cdot \eta + 2 \cdot \pi \cdot V_{out(\min)} \sqrt{L_{lk} \cdot C_{spar}}}. \quad (6)$$

Turns ratio should be increased and D − minimized as long as the primary-side transistors' steady-state voltage stress equals Vout /n. Therefore, it is important to optimize the resonant frequency ωres or the transformer leakage inductance Llk. thus reduced the total equivalent capacitance (Cspar). Fig. 5 displays the Cspar and Llk boundary values for reducing Dmin.

These parameters are approximated at Cspar = 1 nF and Dmin = 0.021 based on the case study output and input voltages and the expected transformer leakage inductance of Llk = 5 µH and n = 0.97 computed with (6).

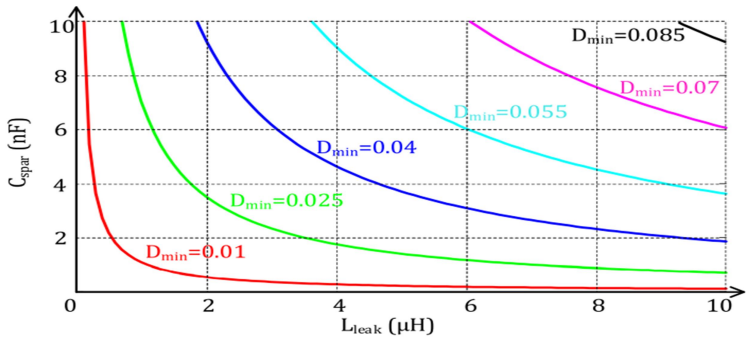


Fig 5 : The relationships among the transformer leakage inductance (Lleak), the minimal duty cycle (Dmin), and the capacitance of S5–S8 (Cspar)

The transistor and transformer currents during the intervals t34 and t45 have no effect on the resonant angular frequency ωres, which is significantly higher than the switching ωsw, ωres >> ωsw. based on the current RMS values. As a result, they can be calculated similarly to traditional current-source inverters.The transformer primary winding current's root mean square (RMS) value is ITXpri.

$$I_{TXpri(RMS)} = \frac{I_{g(\max)} \cdot V_{g(\max)} \cdot n}{V_{out}} \sqrt{\frac{1}{\pi} \cdot \int_0^{\pi} \sin(\varphi)^4 d\varphi}$$

$$= \sqrt{\frac{3}{2}} \cdot \frac{I_{in(\max)} \cdot V_{in(\max)} \cdot n}{2 \cdot V_{out}}. \quad (7)$$

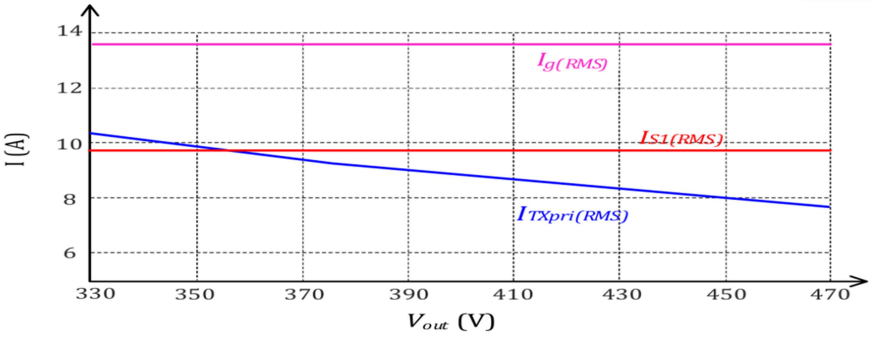


Fig 6: Dependency between maximum input current Ig(RMS) vs. output voltage at constant output power, main transistor S1 RMS current IS1(RMS), and transformer primary winding RMS current ITXpri(RMS).

where the basic angular frequency is represented by the grid angle ϕ.The transistors S1–S4's rms current (IS1–S4rms) is equivalent.

$$I_{S1-S4(RMS)} = \sqrt{\frac{1}{2\pi} \cdot \int_0^{\pi} \left(I_{g(\max)} \cdot \sin(\varphi)\right)^2 d\varphi} = \frac{1}{2} \cdot I_{g(\max)}. \quad (9)$$

The following formula is used to determine the rms current of the transistors S5–S8 (IS5–S8(RMS)):

$$I_{S5-S8(RMS)} = \frac{I_{TXpri(RMS)}}{\sqrt{2} \cdot n} = \frac{\sqrt{3} \cdot I_{g(max)} \cdot V_{g(max)}}{4 \cdot V_{out}}. \quad (10)$$

The currents ITXpri(RMS) and ILlk(max) as a function of the output voltage are displayed in Figure 6. These data might be used to calculate the currents in transistors S1 through S8, which could then be used to construct transformers and choose transistors.

The required THD value, which is dependent on the battery voltage and charging current, should be used to size the input inductor Lin. It goes without saying that when the state of charge rises, the current pulsations grow as well, aggravating the THD, especially in the CV mode. On the other hand, the grid is not greatly affected by the CV mode because of its modest power consumption. Determining the Lin value for adequate THDmax in the CP mode is hencethe objective.

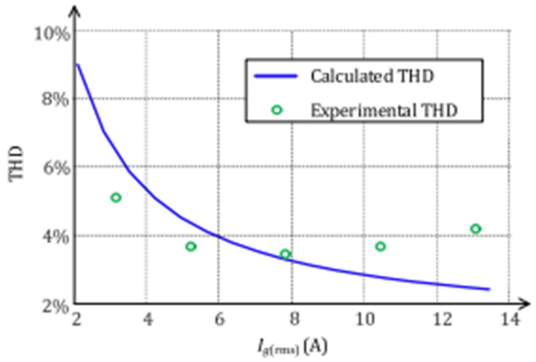


Figure 7 illustrates the relationship between THD and input current at Vout = 400 V.

$$I_g(\varphi) = I_{g(max)} \cdot \sin(\varphi) + I_{dist}(\varphi). \quad (11)$$

THD is computed for such an input current model as follows.

$$THD = \frac{\sqrt{2} \cdot I_{dist(RMS)}}{I_{in(max)}}, \quad (12)$$

where Idist(RMS), which is displayed at the bottom of this page, is the ripple current's rms value as determined by applying formula (13). Fig. 7 displays the theoretical values for Vout = 400 V. At the conclusion of the CP mode, at the maximum voltage of the battery Vout(max), where the current pulsation reaches its maximum value—which might be computed as indicated in (14) at the bottom of this page—the input inductor is calculated for the specified THDnom value. The inductance value equal to Lin = 1.8 mH is calculated from (14) for the situation with a minimum amplitude of the grid current Iin(max) = 16.7 A, Vout(max) = 470 V, Vin(max) = 357 V, and THDnom = 3%.

C. Limitations on Soft-Switching

A number of requirements must be fulfilled for the converter to operate correctly. As previously stated, the ZCS is given when During t34, the primary side's current achieves the instantaneous input current value, or

ip. By changing the duty cycles of the main transistors S1, S2, and t34, the duration of the signal may be modulated.

$$I_{dist(RMS)} = \sqrt{\frac{2}{\pi}\cdot\left(\int_0^{\pi/2} I_{dist}(\varphi)^2 d\varphi\right)} = \sqrt{\frac{2}{\pi}\cdot\left(\frac{1}{12}\cdot\int_0^{\pi/2}\left(\frac{V_{g(\max)}\cdot\sin(\varphi)}{L_{in}}\left(1-\frac{V_{g(\max)}\cdot\sin(\varphi)n}{V_{out}}\right)\cdot T_{sw}\right)^2 d\varphi\right)} = \frac{T_{sw}\cdot V_{g(\max)}\sqrt{9\cdot n^2\cdot\pi\cdot V_{g(\max)}^2 - 64\cdot n\cdot V_{g(\max)}\cdot V_{out} + 12\cdot\pi\cdot V_{out}^2}}{12\cdot\sqrt{2\pi}\cdot L_{in}\cdot V_{out}} \quad (13)$$

$$L_{in} = \frac{T_{sw}\cdot V_{g(\max)}\sqrt{9\cdot n^2\cdot\pi\cdot V_{g(\max)}^2 - 64\cdot n\cdot V_{g(\max)}\cdot V_{out} + 12\cdot\pi\cdot V_{out(\max)}^2}}{12\cdot\sqrt{\pi}\cdot V_{out(\max)}\cdot I_{in(\max)}\cdot THD_{nom}} \quad (14)$$

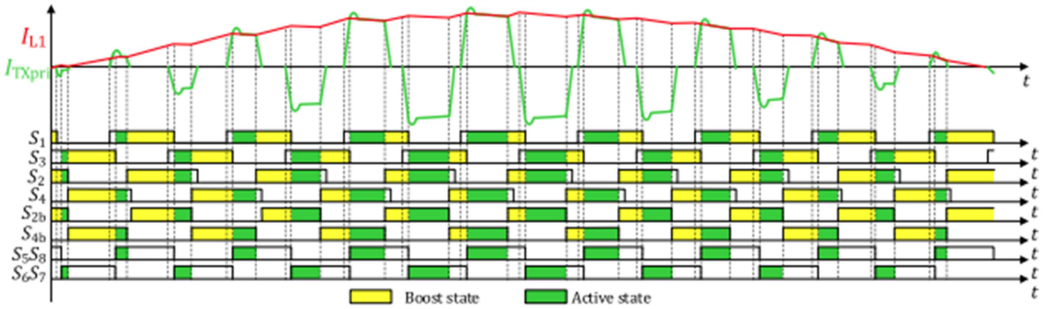
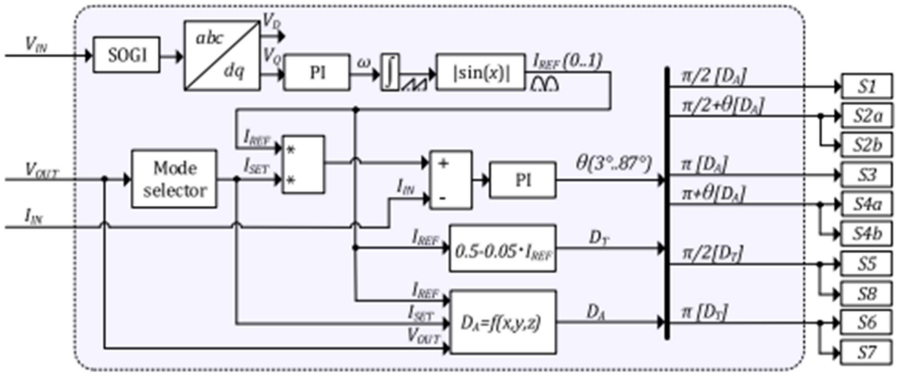


Figure 8: shows the theoretical waveforms of the suggested converter together with the theoretical switching states of transistors.



$$D_A \approx \frac{1}{2} + \frac{2\cdot n\cdot i_p\cdot L_{lk}}{V_{out}\cdot T_{sw}}. \quad (15)$$

The period of Cspar's recharging must be included in the duty cycles of the secondary devices S5–S8:

$$D_T < \frac{1}{2} - \frac{t_{45}}{T_{sw}}. \quad (16)$$

The duty cycle of the transistors S2b and S4b, which are used in the synchronous rectification mode, can be maintained at 0.5. Furthermore, using (7), the minimal phase shift angle needs to be adjusted in line with Dmin.

The converter will function as intended as long as the previously mentioned requirements are met, allowing for the soft turn-off of the secondary devices, zero voltage switching (ZVS), and ZCS of the primary devices.

D. Method of Control

Fig. 8 displays the generalized switching waveforms across the grid frequency half-period. Simple phase-shift modulation is employed to shape the waveform of sinusoidal current. Three input signals are used by the charger's control system: output voltage, reference input current, and grid voltage. In Fig. 9, the control system is shown. A second-order generalized integrator phase lock loop (SOGI PLL) is used to process grid voltage data in order to obtain the grid's fundamental frequency and angle. Normalized unipolar half-sine reference IREF is produced using the collected data. The CP or CV mode is chosen based on the battery voltage measurement. This provides the necessary peak current value ISET, which is multiplied by the normalized reference. The resulting reference is compared with the measured current, and the obtained error signal is processed by the PI controller. The controller output is the phase-shift angle θ between current-side bridge switches, which defines the shoot-through D corresponding to the interval t1 — t5. The phase-shift angle limits are applied based on (7). The resulting phase-shift angle from the controller and normalized reference information are used in the PWM generation to provide circulating energy regulation over the grid period. The phase-shift between the input bridge upper transistors and output bridge remains constant, while the phase-shift of the four-quadrant switches S2 and S4 is varying. The switches S2b and S4b operate in the synchronous rectification mode and could be gated complementary to S4A and S2A, respectively.

The duration of the required induced pulse for implementing the soft-switching feature depends on many factors according to (3) and (4). For the converter parameters listed in Table II and Table III, the duty cycle of the shoot-through state, hence the duty of the soft-switching pulse is simplified as

$$D_A = \frac{2 + I_{SET}/4 + I_{REF}\left(I_{SET}/1.2 + (470 - V_{OUT})/14\right)}{3000}. \quad (17)$$

The carrier wave timer period counter used in the MCU timer peripheral is the same as the denominator. The rotational schedule of primary devices is varying over the input voltage period together with phase-shift angle, which makes the soft-switching current pulse slightly higher than the steady-state transformer current. The dead-time of the secondary devices is also slightly varying depending on the instantaneous input voltage.

TABLE – 3 COMPONENT PARAMETERS

Component	Symbol	Value/Type
Input diode bridge	$D_1 - D_4$	90EPF06L
Primary side transistors	$S_1 - S_{4X}$	UJ3C120080K3S
Secondary side transistor	$S_5 - S_8$	MS 035SMA070B
Filter capacitor	C_0	EZP-E50306MTA
MCU		TMS320F28335
Voltage sensors		AMC1200D
Current sensor		LTS-6-NP
Magnetics		
Input inductor L_{IN}	Core L_{IN}	T300-52D(x2) 1.7 m. H
Transformer TX	Core	R63/38/25(x2), N87
Turns ratio	$N_1 : N_2$	1.03:1
Leakage inductance	L_{lk}	3.8 μH
External snubber cap		680 pF

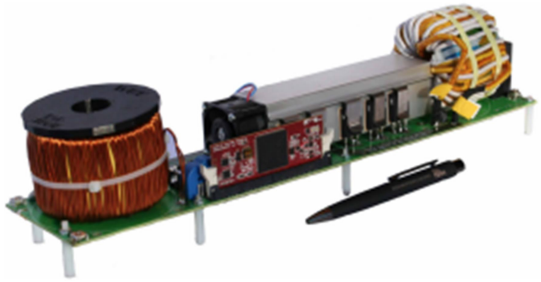


Figure 10: A 3 kW asymmetrical secondary modulated AC-DC converter prototype.

IV. EXPERTIAL RESULTS AND HARDWARE PROTOTYPE

To validate the above-mentioned theoretical analysis and topological functioning, a 3-kW OBC prototype (Fig. 10) was constructed. Tables II and III include a list of the essential converter parts and converter parameters. The transformer turns ratio is selected such that, when the maximum grid voltage of 253 VAC is provided to the converter's input, the OBC may operate at the minimum output voltage of 330 VDC.

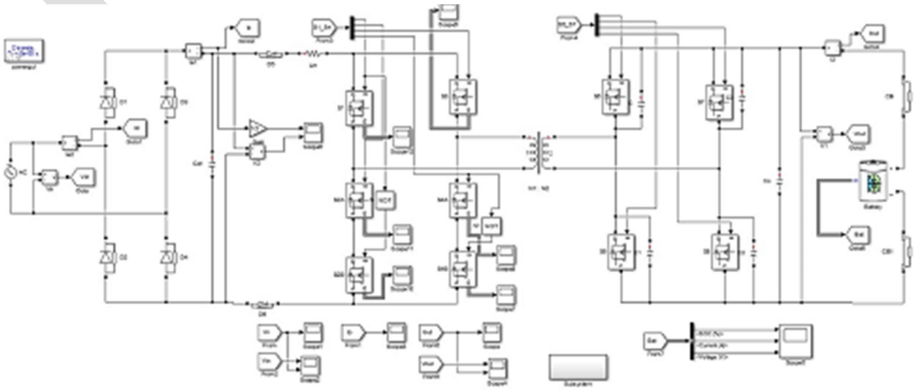


Figure 11. Simulink Diagram

To build the input inductor, two T300-52D torpid powder cores from Micro metals were used. Two paralleled layers of solid copper wire, the inner and outer, are accommodated in the winding. 1.5 and 1.25 mm in diameter, respectively. Fig. 11 displays the resultant inductance characteristics. Figure 12 shows the reference step response (c) of the input current and validates the suggested converter's performance for partial (a) and full (b) loads. The harmonic distortion criteria, which call for a THD of less than 5%, are satisfied by the existing waveforms (see Fig. 7). The THD marginally increases near the rated power when the inductance value drops because of the nonlinear feature of the powder core input inductance (see Fig. 11).

The transformer voltage and current waveforms during a single switching period are displayed in Figs. 14(a) and (b). In contrast to the majority of resonant converters, the transformer's current during Low total rms current stress is the outcome of the boost mode equaling zero and no circulating current appearing. The voltage and current waveforms of the switch S1 operating at the rated output power and Vout = 400 V close to the sine peak are displayed in Fig. 14(c). The transformer's leakage inductance limits the current increase rate during the transistor turn-on transient, which also lowers the associated power loss. The ZCS is operational as evidenced by the current across the switch dropping to zero just before the turn-off. Throughout the duration of the grid period, these soft-switching qualities are preserved.

The ZCS action of the transistor S2A as a result of its current declining to zero is shown in Fig. 15(a). Waveforms of voltage and current are seen across the switches S5–S8 at the sine peak and Fig. 15(c) at around 50% of the grid voltage's sine amplitude. The transistors function in the synchronous rectification mode when they are in the active state. The opposing polarity's current pulse may be seen at the conclusion of the on-state interval. Its amplitude, which permits the major bridge switches to operate with ZCS, is determined by the duration of t34.

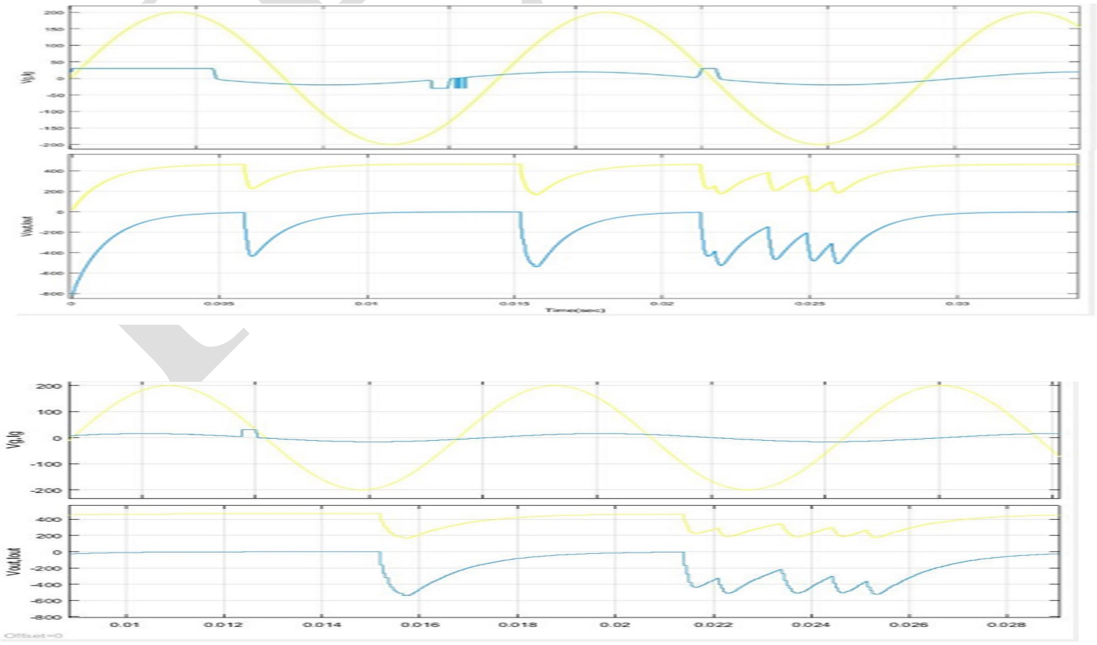
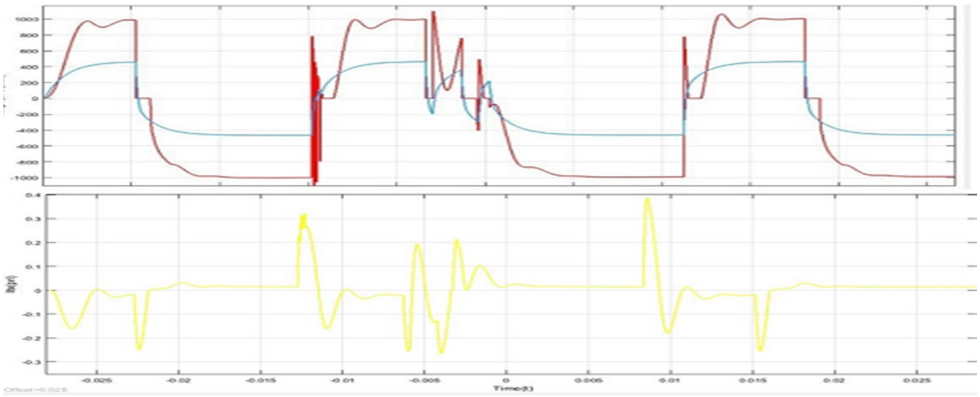


Figure 12. (a) Voltage and current of input and output converters operating at low load Pin=0.8 kW, Vout=400 V; (b) The voltage and current of the input and output converters while operating at full load Pin=3 kW, Vout=400 V;

(C) Dynamic response of the conv



erter reference step-up at Vout=400 V

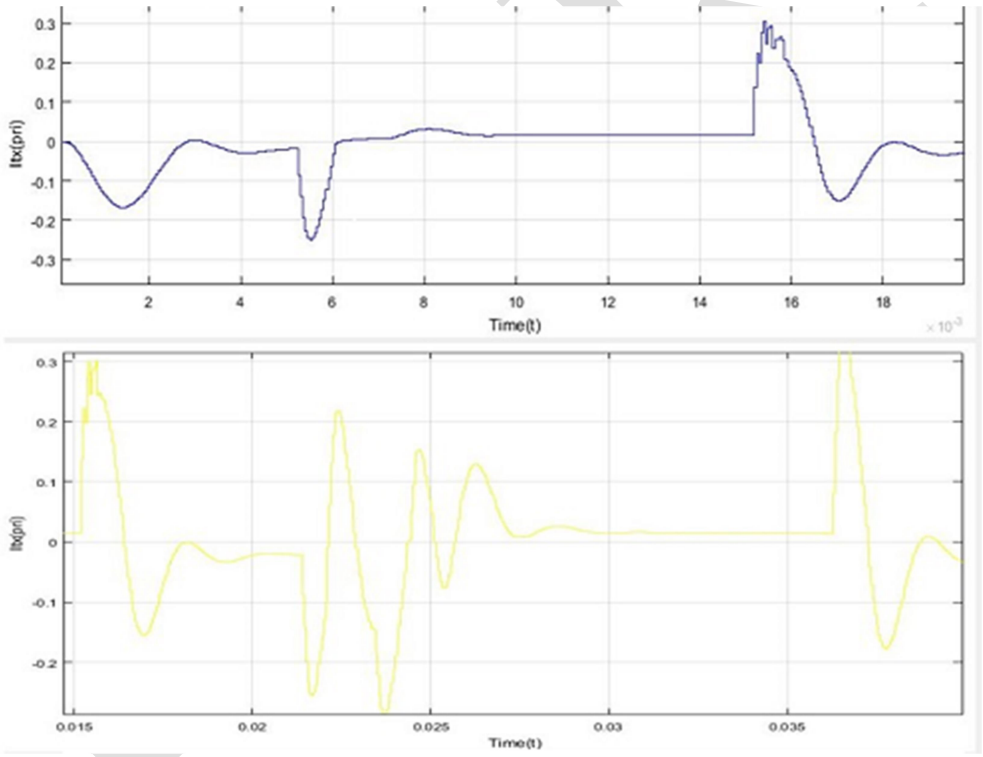


Figure 13: shows the input and output converter voltage and current under full load conditions. (a) Pin=3kW at Vout=330V and at; (b) Vout=470V; and (c) Input converter voltage and current, transformer main winding current at Pin=3kW at Vout=400V.

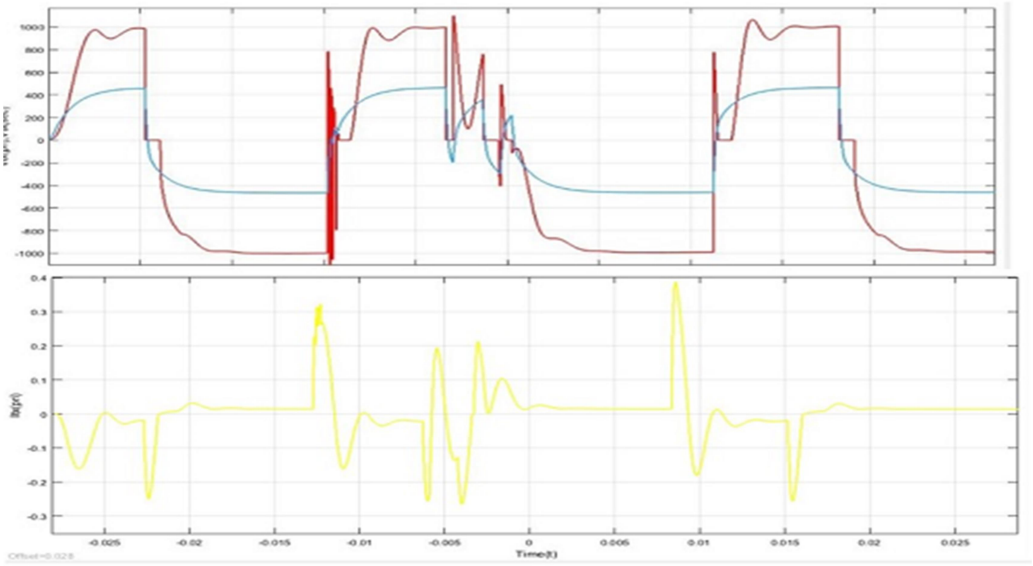


fig. 14: Transformer waveforms at one switching period at: (a) transceiver S1 voltage and current over switching period at Vout = 400 V, Pin = 3 kW at the sine peak at; (b) 50% of the sine amplitude.

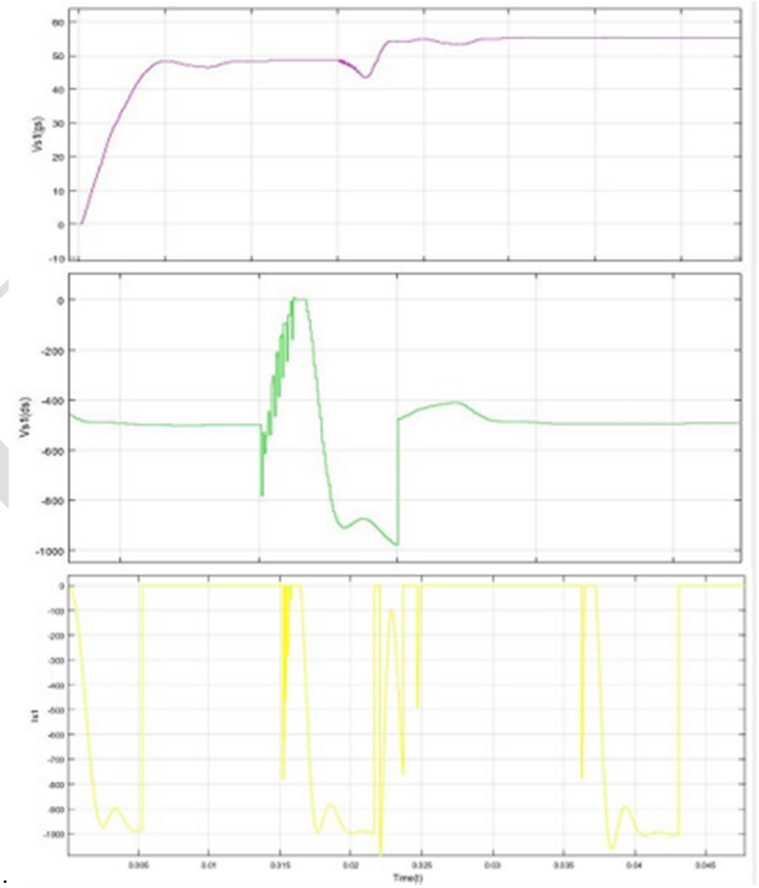


Fig. 15:(a) the switch S1 with ZVS and ZCS is turned on and off; (b) the switch S2A with decreased di/dt and ZCS is turned on and off; and (C) the switch S5 is turned on and reverse.

It was possible to see a fluctuation in the amplitude of the reverse current according to the load current. The precise transients of switch S1, where the ZCS is detected, are displayed in Fig. 16(a). Tiny The turn-on transient starts at the beginning with the appearance of current related to parasitic capacitance. Transients and the ZCS turn-off of the switch S2A are displayed in Fig. 16(b). Figure 16(c) displays the reverse current pulse and the ZVS turn-on transient of switch S5. Figure 17 displays the charger's efficiency characteristics as determined by the Yokogawa WT3000 power analyzer, while Figure 18 displays the predicted breakdown of power loss. At the lowest output voltage, Vout = 330 V, the converter showed the maximum efficiency; the output voltage declines with the voltage increase. This contrasts with the rival OBC methods, where a reverse efficiency trend was seen [14], [31], meaning that the maximum output voltage is obtained at the maximum efficiency. It usually corresponds to a CV operating mode. Generally speaking, the CP mode should handle the majority of the power used throughout the charging process. Consequently, the total weighted charging efficiency rating is less affected by the efficiency characteristic in the CV mode. In addition, it is often advised to maintain a battery's charge between 20 and 80% in order to extend its lifespan [25]. Following this advice would result in the CV charging mode happening very infrequently. This demonstrates that the battery charging profile should ideally be considered when evaluating the charger's efficiency.

To assess the charging performance of the converter, the efficiency versus the state-of-charge curve for different reference converters is depicted in Fig. 19. The battery voltage is normalized according to the maximum output voltage of a particular OBC. It is assumed that each OBC operates at the rated power during the CP mode, while the power is reduced in the CV mode. Evidently, the non-isolated configuration [10] demonstrated the highest efficiency potential. However, such solutions have not been yet adopted in the industry due to touch currents and safety issues [12]. The proposed isolated single-stage charger demonstrated the charging characteristic close to the state-of-the art two-stage system [32] during the CP modeEven though efficiency is reduced in the CV mode, both the total processed energy and the impact on overall efficiency are negligible. This demonstrates that the suggested single-stage topology's reasonably straightforward control, lack of a large DC-link capacitor, and excellent charging performance qualify it for authorized permitted usage restricted to attractive as OBC.

V. SUMMARY

Using the advantages of the single-stage AC-DC current source converter, this article presented one for the OBC application. Conversion of energy. A 3 kW prototype was used to demonstrate and experimentally validate the design guidelines. PFC functionality was put into practice by applying the straightforward single phase-shift modulation technique. Therefore, low latency sensors and high-performance processors are not necessary for the charger control system to function well. It was shown that the converter's THD does not go over 5%, meeting the requirements of IEC 61000-2-2. Experimental verification of the converter's soft-switching capabilities for the primary and secondary side transistors was conducted. A notable advantage of the topology is the transformer's low RMS currents. The efficiency change trend of the charger is inversely correlated with the output voltage.

REFERENCES

[1] F. Mwasilu, J. Justo, E. K. Kim, T. Do, and J. W. Jung, “Electric vehicles and smart grid interaction: A review on vehicle to grid and renewable energy sources integration.”, Renewable Sustain. Energy Rev., vol. 34. pp. 501–516, 2014 doi: 10.1016/j.rser.2014.03.031.

[2] H. Tu, H. Feng, S. Srdic, and S. Lukic, "Extreme fast charging of electric vehicles: A technology overview," IEEE Trans. Transp. Electrific., vol. 5, no. 4, pp. 861–878, Dec. 2019, doi: 10.1109/TTE.2019.2958709.

[3] M. Yilmaz and P. T. Krein, "Review of battery charger topologies, charging power levels, and infrastructure for plug-in electric and hybrid vehicles," IEEE Trans. Power Electron., vol. 28, no. 5, pp. 2151–2169, May 2013, doi: 10.1109/TPEL.2012.2212917.

[4] D. S. Gautam, F. Musavi, M. Edington, W. Eberle, and W. G. Dunford, "An automotive onboard 3.3-kW battery charger for PHEV application," IEEE Trans. Veh. Technol., vol. 61, no. 8, pp. 3466–3474, Oct. 2012, doi: 10.1109/TVT.2012.2210259.

[5] S. Kim and F. Kang, "Multifunctional onboard battery charger for Plug-in electric vehicles," IEEE Trans. Ind. Electron., vol. 62, no. 6, pp. 3460–3472, Jun. 2015, doi: 10.1109/TIE.2014.2376878.

[6] H. Wang and Z. Li, "A PWM LLC type resonant converter adapted to wide output range in PEV charging applications," IEEE Trans. Power Electron., vol. 33, no. 5, pp. 3791–3801, May 2018, doi: 10.1109/TPEL.2017.2713815.

[7] S. Ryu, D. Kim, M. Kim, J. Kim, and B. Lee, "Adjustable frequency–dutycycle hybrid control strategy for full-bridge series resonant converters in electric vehicle chargers," IEEE Trans. Ind. Electron., vol. 61, no. 10, pp. 5354–5362, Oct. 2014, doi: 10.1109/TIE.2014.2300036.

[8] H. Wang, S. Dusmez, and A. Khaligh, "Design and analysis of a fullbridge LLC-Based PEV charger optimized for wide battery voltage range," IEEE Trans. Veh. Technol., vol. 63, no. 4, pp. 1603–1613, May 2014, doi: 10.1109/TVT.2013.2288772.

[9] F. Jauch and J. Biela, "Combined phase-shift and frequency modulation of a dual-active-bridge AC–DC converter with PFC," IEEE Trans. Power Electron, vol. 31, no. 12, pp. 8387–8397, Dec. 2016, doi: 10.1109/TPEL.2016.2515850.

[10] C. Oh, D. Kim, D. Woo, W. Sung, Y. Kim, and B. Lee, "A high-efficient nonisolated single-stage on-board battery charger for electric vehicles," IEEE Trans. Power Electron., vol. 28, no. 12, pp. 5746–5757, Dec. 2013.

[11] A. Khaligh and M. D'Antonio, "Global trends in high-power on-board chargers for electric vehicles," IEEE Trans. Veh. Technol., vol. 68, no. 4, pp. 3306–3324, Apr. 2019.

[12] S. Rivera, S. Kouro, S. Vazquez, S. M. Goetz, R. Lizana, and E. RomeroCadaval, "Electric vehicle charging infrastructure: From grid to battery," IEEE Ind. Electron. Mag., vol. 15, no. 2, pp. 37–51, Jun. 2021, doi: 10.1109/MIE.2020.3039039.

[13] S. Jeong, Y. Jeong, J. Kwon, and B. Kwon, "A soft-switching single-stage converter with high efficiency for a 3.3-kW onboard charger," IEEE Trans. Ind. Electron., vol. 66, no. 9, pp. 6959–6967, Sep. 2019, doi: 10.1109/TIE.2018.2877093.

[14] M. Kwon and S. Choi, "An electrolytic capacitorless bidirectional EV charger for V2G and V2H applications," IEEE Trans. Power Electron., vol. 32, no. 9, pp. 6792–6799, Sep. 2017, doi: 10.1109/TPEL.2016.2630711.

[15] C. Li, Y. Zhang, Z. Cao, and D. Xu, "Single-Phase single-stage isolated ZCS current-fed full-bridge converter for high-power AC/DC applications," IEEE Trans. Power Electron., vol. 32, no. 9, pp. 6800–6812, Sep. 2017, doi: 10.1109/TPEL.2016.2623771.

[16] U. R. Prasanna, A. K. Singh, and K. Rajashekara, "Novel bidirectional single-phase single-stage isolated AC–DC converter with PFC for charging of electric vehicles," IEEE Trans. Transp. Electrific., vol. 3, no. 3, pp. 536–

544, Sep. 2017, doi: 10.1109/TTE.2017.2691327.

[17] H. Belkamel, H. Kim, and S. Choi, "Interleaved totem-pole ZVS converter operating in CCM for single-stage bidirectional AC–DC conversion with high-frequency isolation," IEEE Trans. Power Electron, vol. 36, no. 3, pp. 3486–3495, Mar. 2021.

[18] A. Blinov, R. Kosenko, A. Chub, and D. Vinnikov, "Bidirectional soft switching current source DC-DC converter for residential DC microgrids," in Proc. IECON - 44th Annu. Conf. IEEE Ind. Electron. Soc., Washington, DC, USA, 2018, pp. 6059–6064, doi: 10.1109/IECON.2018.8591103.

[19] US Department of Energy, energy efficiency and renewable energy, "Advanced vehicle testing – Beginning-of-Test battery testing results, 2011 Nissan Leaf – VIN 0356" U.S Department of Energy, Tech. Rep., Accessed: Sep. 30, 2021. [Online]. Available: http://media3.ev-tv.me/ DOEleaftest.pdf

[20] L. Lam and P. Bauer, "Practical capacity fading model for Li-Ion battery cells in electric vehicles," IEEE Trans. Power Electron., vol. 28, no. 12, pp. 5910–5918, Dec. 2013, doi: 10.1109/TPEL.2012.2235083.

[21] W. W. Chen, R. Zane, and L. Corradini, "Isolated bidirectional grid-tied three-phase AC–DC power conversion using series-resonant converter modules and a three-phase unfolder," IEEE Trans. Power Electron., vol. 32, no. 12, pp. 9001–9012, Dec. 2017.

[22] J. Rabkowski, A. Blinov, D. Zinchenko, G. Wrona, and M. Zdanowski, "Grid-frequency Vienna rectifier and isolated current-source DC-DC converters for efficient off-board charging of electric vehicles," in Proc. 22nd Eur. Conf. Power Electron. Appl., 2020, pp. P.1–P.10. [23] A. Tausif, H. Jung, and S. Choi, "Single-stage isolated electrolytic capacitor-less EV onboard charger with power decoupling," CPSS Trans. Power Electron. Appl., vol. 4, no. 1, pp. 30–39, Mar. 2019. [24] A. Ghassemi, P. C. Banerjee, Z. Zhang, A. Hollenkamp, and B. Bahrani, "Aging effects of twice line frequency ripple on lithium iron phosphate (LiFePO4) batteries," in Proc. 21st Eur. Conf. Power Electron. Appl., Genova, Italy, 2019, pp. P.1–P.9.

[25] M. J. Brand, M. H. Hofmann, S. S. Schuster, P. Keil, and A. Jossen, "The influence of current ripples on the lifetime of lithium-ion batteries," IEEE Trans. Veh. Technol., vol. 67, no. 11, pp. 10438–10445, Nov. 2018.

[26] L. Chen, S.Wu, D. Shieh, and T. Chen, "Sinusoidal-ripple-current charging strategy and optimal charging frequency study for Li-Ion batteries," IEEE Trans. Ind. Electron., vol. 60, no. 1, pp. 88–97, Jan. 2013.

[27] S. Bala, T. Tengnér, P. Rosenfeld, and F. Delince, "The effect of low frequency current ripple on the performance of a lithium iron phosphate (LFP) battery energy storage system," in Proc. IEEE Energy Convers. Congr. Expo., 2012, pp. 3485–3492.

[28] A. Blinov, I. Verbytskyi, D. Zinchenko, D. Vinnikov, and I. Galkin. [Modular battery charger for light electric vehicles,] Energies, vol. 13, no. 4, pp. 774, 2020. [Online]. Available: https://doi.org/10.3390/en13040774

[29] M. R. Ahmed, R. Todd, and A. J. Forsyth, "Predicting SiC MOSFET behavior under hard-switching, soft-switching, and false turn-on conditions," IEEE Trans. Ind. Electron., vol. 64, no. 11, pp. 9001–9011, Nov. 2017. Authorized licensed use limited to: VISVESVARAYA NATIONAL INSTITUTE OF TECHNOLOGY. Downloaded on September 28,2022 at 11:59:38 UTC from IEEE Xplore. Restrictions apply. 12592 IEEE TRANSACTIONS ON VEHICULAR TECHNOLOGY, VOL. 70, NO. 12, DECEMBER 2021

[30] A. Blinov, V. Ivakhno, V. Zamaruev, D. Vinnikov, and O. Husev, "Experimental verification of DC/DC converter with full-bridge active rectifier," in Proc. IECON - 38th Annu. Conf. IEEE Ind. Electron. Soc., 2012, pp. 5179–5184.

[31] Z. Zhang et al., "Analysis and design of a single-stage bridgeless isolated AC-DC resonant converter for programmable AC power source applications," IEEE Access, vol. 8, pp. 219071–219082, 2020, doi: 10.1109/ACCESS.2020.3042541.

[32] C. Wei, D. Zhu, H. Xie, and J. Shao, "A 6.6kW high power density bi-directional EV on-board charger based on SiC MOSFETs," in Proc. PCIM Europe; Int. Exhib. Conf. Power Electron., Intell. Motion, Renewable Energy Energy Manage., 2019, pp. 246–252.

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