BETTER DC-DC CONVERTERS WITH HYBRID SWITCHED INDUCTOR/SWITCHED CAPACITOR

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ABSTRACT: Elevated voltage increase DC-DC converters are widely utilized in many different applications, such as sustainable low-voltage sources. Due to the use of a high duty cycle ratio, conventional boost converters have low efficiency, high voltage stress, and high current ripple, which restrict their voltage gain. In this study, we propose converters consisting of four sub-structures: an auxiliary switch with non-isolated configuration, an active switched inductor, a passive switched inductor, and a switched capacitor cell. In addition to having a low duty cycle ratio, the suggested structures have a significant voltage gain when compared to the traditional ones that are either switched capacitor- or inductor-based. Efficiency is increased with the addition of an auxiliary switch, especially for high voltage gains. A detailed discussion is given of the operation concept and steady-state analysis. Additionally, a prototype constructed for experimental analysis validates the simulation results from the PSCAD/EMTDC program. The findings show that using the auxiliary switch could increase the voltage gain and efficiency.

I.INTRODUCTION

These days, low voltage sources are used to achieve high output voltage levels by the use of DC-DC converters with high voltage gain [1]. Among other converters, DC-DC boost converters seemed appropriate for these uses. Nevertheless, when the duty cycle approaches unity in these converters, the voltage gain is constrained by higher conduction losses. Furthermore, efficiency, reverse recovery, and electromagnetic interference may be impacted by a greater duty cycle ratio [2]–[4]. Furthermore, high voltage components are needed for high voltage gain, which raises switching and conduction losses [5, 6]. Another restriction on a step-up voltage increase is the equivalent series resistance of the elements [7].

In several converter types, including push-pull, forward, fly back, full-bridge, and half-bridge, high voltage gain can be obtained by varying the transformer's turns ratio. However, the transformer's leakage inductor in these converters results in strong voltage spike and high power dissipation [1, 7, 8]. A half-bridge fly back converter with a novel lossless passive snubber was presented in [9] utilizing an interleaved construction in order to get around these issues. In order to achieve soft-switching conditions for all semiconductor elements at turn-on/off states, the authors in [10] also proposed a passive lossless snubber. To achieve high efficiency and cheap cost, non-isolated DC-DC converters were designed to eliminate the transformer's leakage inductance. These converters fall into one of two categories: coupled or non-coupled inductor [11]. Non-coupled inductor type can reduce both the number and size of magnetic components [12]–[15]. A composite approach based on the use of many capacitors in switching-mode DC-DC converters was put out in [16]. One can anticipate great efficiency because of the low duty cycle and strong voltage gain introduced in [16]. A switched capacitor circuit that uses numerous capacitors to enable a wide range of output voltage was integrated with a boost converter in [17]. For constant voltage, the combined structure's efficiency is low [17].

Non-isolated DC-DC converters were created with the purpose of removing the leakage inductance from the transformer in order to attain high efficiency at a low cost. There are two types of these converters: connected inductor and non-coupled inductor [11]. The number and size of magnetic components can be decreased by using non-coupled inductors [12]–[15]. In switching-mode DC-DC converters, a composite solution based on the employment of many capacitors was published in [16]. Because of the substantial voltage gain and short duty cycle established in [16], one might expect great efficiency. In [17], a boost converter was combined with a switched capacitor circuit that makes use of many capacitors to provide a broad range of output voltage. The efficiency of the combined construction is low for constant voltage [17].

This study presents the addition of an auxiliary switch to the standard hybrid switched inductor/switched capacitor converters in order to reduce the duty cycle ratio and increase practical voltage gain [5], [19]. Accordingly, an auxiliary switch has been incorporated with three widely used switched capacitor switched inductor active network converter (SC-SL-ANC), symmetrical hybrid switched inductor (SH-SL), and asymmetrical hybrid switched inductor (AH-SL) architectures. The kept Energy levels of the inductor and capacitor are raised to supply the simply including the auxiliary switch, you can add a load without creating a second clamping circuit. In fact, substantial voltage gain can be achieved by the suggested converters without the need for additional hybrid switching capacitors [14] or hybrid capacitor approaches [15]. Additionally, the suggested converters' efficiency is significantly higher than that of earlier designs for the same voltage increase.

This is how the rest of the paper is structured. The suggested converters' structure is shown in Section II. Within Section III provides an explanation of the converters' working principles. In Section IV, the theoretical voltage gains are computed. The suggested structures are covered in full in Section V. Additionally, in Section VI, the suggested converters are contrasted with comparable converters. Section VII provides simulation and experimental analysis. The final section of this paper is the conclusion.

II. THE PROPOSED CONVERTERS' STRUCTURAL DESIGN

This paper presents the development of three converters using a combination of an auxiliary switch, an active switched inductor (ASL) network [5], a passive switched inductor (PSL) network [5], and a switched capacitor (SC) cell [1]. Fig. 1 depicts the proposed converters' structural layout. Two sub-structures, the hybrid asymmetrical switched inductor (HASL) and the hybrid symmetrical switched inductor (HSSL), are produced when ASL and PSL networks are combined. An auxiliary switch and a HASL make up the improved asymmetrical hybrid switched inductor (IAH-SL) converter (Fig. 1(a)). Fig. 1(b) shows the improved symmetrical hybrid switched inductor (ISH-SL), which is made up of an auxiliary switch and an HSSL. Additionally, the enhanced symmetrical hybrid switched inductor switched capacitor (ISH-SL-SC) is composed of an auxiliary switch, a SC-cell, and HSSL.

III. ANALYSIS OF OPERATIONS

This section discusses the operating principle and steady-state analysis of the suggested architectures for continuous conduction mode (CCM), as seen in Fig. 2.It is assumed that every component is perfect in order to streamline the analysis. Additionally, the behaviours of resistors, capacitors, and inductors are linear, time-invariant, and frequency independent. The three converters' switching processes are comparable, thus we just need to examine the ISH-SL-SC operating modes.

[0 ≤ t < D1Ts] is Mode 1. In this manner, the switches S1, S2, and S3 are all switched off simultaneously, as shown in Fig. 2(a). Inductors L1a, L2a, L1b, and L2b see a linear rise in current when connected in parallel to Vin. Through the S1, S2, and stored energy in C3 from the previous mode, the capacitor C1 is charged. The diodes D1a, D1c, D2a, D2c, and D4b are activated in this mode, while the remaining diodes are blocked. The formulas for inductors' voltage and current are (1) and (2). Additionally, (3) and (4) provide the voltages of the switched capacitors C1 and C2 in the SC-cell.

$$V_{L1a}=V_{L1b}=V_{L2a}=V_{L2b}=V_{in} \quad (1)$$

$$\Delta i_{L1a}=\Delta i_{L1b}=\Delta i_{L2a}=\Delta i_{L2b}=(V_{in}\Delta t)/L \quad (2)$$

$$V_{C1}=V_{in}+V_{C3} \quad (3)$$

$$V_{C2}=V_o-V_{C3} \quad (4)$$

D1 D2 Ts t Mode 2 D1 Ts: Fig. 2(b) shows that S1, S2, and S3 switches are off and S3 is switched on. Inductors L1a, L2a, L1b, and L2b have linearly increasing current in series relationship with Vin. In the meantime, the voltage of capacitors C1 and C3 is the same. Furthermore, the inductors current's rising steepness is less than that of Mode 1. Diodes D1b, D2b, D3, and D4b are activated in this mode, while the remaining diodes are blocked. Additionally, inductors' voltage and current values are derived from equations (5) and (6).

$$V_{L1a}=V_{L1b}=V_{L2a}=V_{L2b}=V_{in}/4 \quad (5)$$

$$\Delta i_{L1a}=\Delta i_{L1b}=\Delta i_{L2a}=\Delta i_{L2b}=V_{in}\Delta t/4L \quad (6)$$

D1 D2 Ts t Ts - Mode 3: Fig. 2(c) shows that all of the switches, S1, S2, and S3, are off. On the output load Ro, all of the switched inductors' and switched capacitors' stored energy is released. Diodes D1b, D2b, D4a, and D4c are activated in this mode, while the remaining diodes are blocked. This operation method yields the following equations.

$$V_{L1a}=V_{L1b}=V_{L2a}=(3V_{in}-V_o)/8 \quad (7)$$

$$V_{C1}=V_{C2}=(V_{in}+V_o)/2 \quad (8)$$

$$V_o=V_{C2}+V_{C3} \quad (9)$$

$$V_{C3}=(V_o-V_{in})/2 \quad (10)$$

Figure 3 shows the primary ISH-SL-SC waveforms.

IV. PHOTOGRAPHY OF THE PERFECT CONVERTER

The voltage gain of the suggested ISH-SL-SC converter is shown in this section. This voltage gain is based on the voltage-second balancing of the inductors and is obtained from their operating modes. The limitation in (11) needs to be met in this converter in order to accomplish the intended operation principles.

$$D_1+D_2<1 \quad (11)$$

By using (1), (5), and (7), the voltage gain of ISH-SL-SC in CCM may be calculated using the following equations.

$$8V_{in}D_1+2V_{in}D_2+(3V_{in}-V_o)(1-D_1-D_2)=0 \quad (12)$$

$$\text{Vin=1-D1-D2} \quad (13)$$

V. CAREFUL ANALYSIS AND DESIGN THOUGHTS

First, the structure is broken down into its component parts and examined individually in order to illustrate the functioning features of the ISH-SL-SC that is being discussed in this section. Second, the output capacitor

requirements are established. Thirdly, parasitic elements such as the on-state collector-to-emitter voltage drop VCE−on, switching turning-on losses Eon and turning-off losses Eoff, on-resistance of the switches ron, forward resistance of the diodes rD, the threshold voltage of the diodes VF, equivalent series resistance (ESR) of the inductors rL, and ESR of the capacitors rC are taken into account when calculating the power losses and efficiency of designed converters.

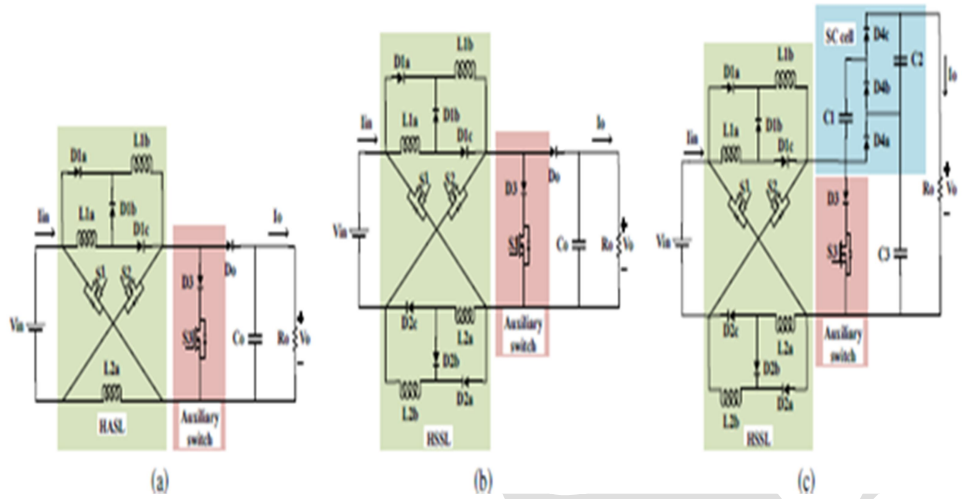

Figure 1 shows the modified converters' structure, which includes an S3 auxiliary switch. IAH-SL (a). (b) ISH-SL. (c) ISH-SL

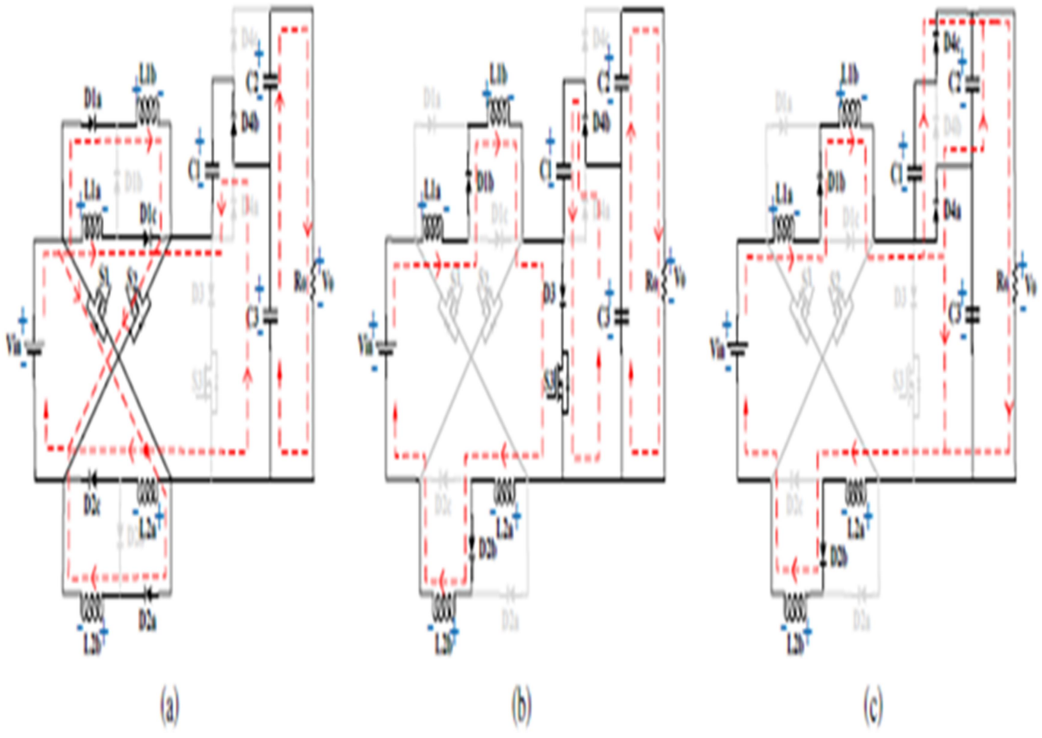

Fig. 2 shows the suggested ISH-SL-SC converter's operating modes. Modes 1 and 2 (a, b, and c)

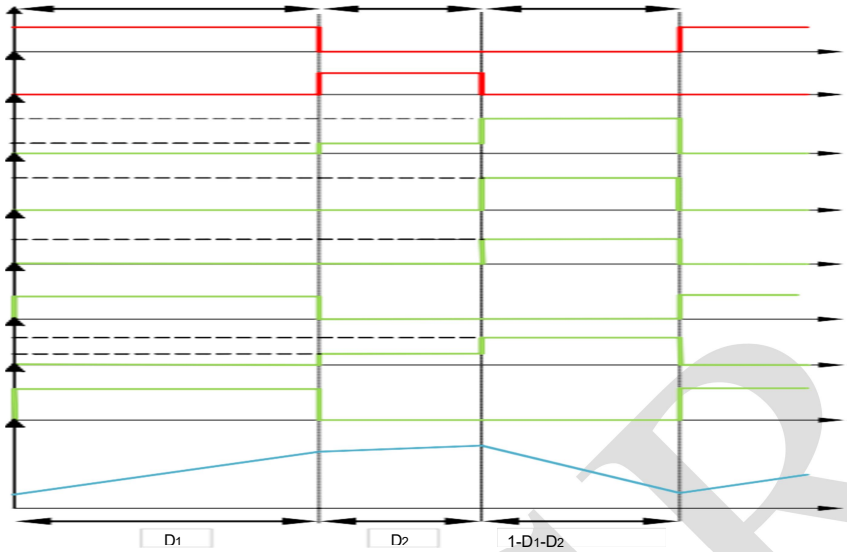

Figure 3: The proposed ISH-SL-SC converter's key operating waveforms

Sub-components of the suggested converters

The planned converter's structure is made up of a combination of auxiliary switch sub-structures, SC cell, and HSSL, as shown in Fig. 1(c). It is important to note that CCM evaluates the design process. Furthermore, it is believed that inductors' current ripple is minimal.

HSSL Inductors L1a, L1b, L2a, and L2b: Vin and the inductor variations charge the inductors during Modes 1 and 2.The currents are ΔiL. Consequently, (14) expresses the value of switched capacitors in the ISH-SL-SC.

$$L = \frac{V_{in}}{4\Delta i1f}\left(4D_1 + D_2\right) \qquad (14)$$

Switches S1, S2: Stresses from voltage and current have an impact on switch design. Thus, the voltage andThe primary switch current stresses are computed using equations (15) and (16).

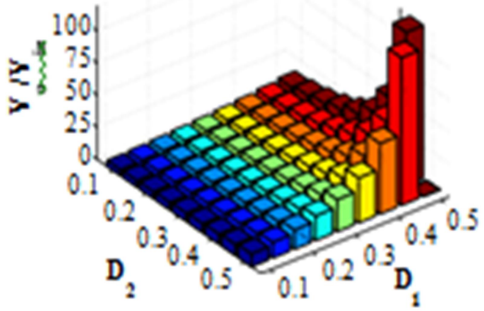

Figure 4 shows the suggested ISH-SL-SC converter's voltage gain.

$$V_{S1S2}^{stre} \qquad (Vo + Vin)\backslash 4 \qquad (15)$$

$$i_{s4s2}^{stress} = (l_{in} + 5l_o)\backslash 4 \quad (16)$$

The most crucial aspects of diode design are voltage and current stresses in diodes D1a,D1b, D1c, D2a, D2b, and D2c.

$$V_{D1a,D1c,D2a,D2c}^{stress} = (Va - |3Vin) \quad (17)$$

$$V_{D1b,D2b,=Vin}^{stress} \quad (18)$$

$$i_{D1a,D1c,D2a,D2c}^{strees} = (L_{in} + 3l_o)\backslash 2 \quad (19)$$

$$i_{D1b,D2b}^{stress} = L_{im} \quad (20)$$

- An additional switchinISH-SL-SCisequaltohalfoftheoutputvoltage

$$V_{S3}^{strees} = V_{o\backslash 2} \quad (21)$$

Furthermore, there is a relationship between the inductor's current and the switch S3's average current. Thus, the subsequent formula is obtained.

$$i_{s3}^{stress} = (l_{in} + 5\backslash o)\backslash 8 \quad (22)$$

Furthermore, D3 experiences the same voltage and current stressors as S3.

SC cell Capacitors C1, C2: Using (23), the average voltage of the switched capacitors is determined by assuming C1 = C2.

$$(Vo + Vin)/2 = VC1,C2 \quad (23)$$

According to (23), the necessary voltage gain has a significant impact on the capacitor's voltage rating.

D4a, D4b, and D4c diodes: The D1, D2 function and the operation principles of SC diodes are connected, as shown in Fig. 2. Therefore, the voltage and current equations below are obtained.

$$V_{D4a,D4b,D4c}^{stress} = V_{o\backslash 2} \quad (24)$$

$$i_{D4a,D4b,D4c}^{stress} = l_o \quad (25)$$

B. Capacitor for output

When S1, S2, or S3 are turned on, the output capacitor's voltage rises sharply (charging), as described in Modes 1 and 2. On the other hand, as said in Mode 3, all switches are off, yet the output voltage has dropped. The electric charge (Q) held in Co is correlated with the output capacitor's value.

$$\Delta VC_0 = \Delta Q\backslash C_0 \quad (26)$$

$$\Delta VC_0 = \frac{V_0 (D_1 + D_2)}{F_{sR_{C0}}} \quad (27)$$

It is important to remember that the ISH-SL-SC output capacitor is equivalent to a series of C2 and C3 (see Fig. 2).

C. Power dissipation and CCM efficiency

In (29)–(53), the ripple-free current of the inductors is assumed in order to determine the efficiency of ISH–SL–SC. Therefore, (29) and (30), respectively, simulate the conduction losses for IGBT and MOSFET.

$$(P)^{IGBT} = \text{VCE} - onIs\ avg \quad (28)$$

$$(\text{Ds} - \text{con})^{MOSFET} = R\ I^2 \quad (29)$$

Accordingly, (31) and (32), for IGBT and MOSFET, respectively, simulate the switching losses PS sw.

$$P_{S-5W}^{(GB)} = (F - - + E_{off)f_s} \quad (31)$$

$$P_{S-5W}^{MOSFET} = (F_{SC}{}^{SW\ V\ \frac{2}{S})2} \quad (32)$$

$$P_{S=\ P_{CON+}P_{SW}} \quad (33)$$

$$P_{rD\ =r_{D\ i^2\ rms}} \quad (34)$$

$$P_{VF\ =\ V_{F\ I}D\ ave} \quad (35)$$

By taking into account equations (34) and (35) the total diode conduction losses are found using equation (36).

Structure/ Ref.	Voltage Gain	Normalized Voltage stress (G=V_o/V_{in})		No. of Components			
		Switch	Diode	S	D	L	C
ISH-SL-SC	(5D1 -D2 +3)/(1-D1 -D2)	(G+1)/4	(G-1)/8	3	10	4	3
ISH-SL	(3D1 -D2 +1)/(1-D1 -D2)	(G+1)/2	(G-1)/4	3	8	4	1
IAH-SL	(2D1 +1)/(1-D1 -D2)	(2G+1)/3	(G-1)/3	3	5	3	1
AH-SL [5]	(2D+1)/(1-D)	(2G+1)/3	(G-1)/3	2	4	3	1
SH-SL [5]	(3D+1)/(1-D)	(G+1)/2	(G-1)/4	2	7	4	1
SC-ANC [14]	(D+2)/(1-D)	(G+1)/4	(G+1)/4	2	3	2	3
SL-ANC [14]	(2D+1)/(1-D)	(D+3)/(1-D)	(D+3)/(1-D)	2	3	4	1
SC-SL-ANC [19]	(5D+1)/(1-D)	(G+1)/4	(G-1)/8	2	9	4	3
SL/SC-SBC [15]	2(1-D)/(1-3D)	2D/(1-3D)	2D/(1-3D)	2	7	2	3
ASL-SU2C [1]	(3D+1)/(1-D)	1/(1-D)	2/(1-D)	2	2	3	3
HBC [25]	(3-D)/(1-D)	1/(1-D)	1/(1-D)	1	5	1	4
HSXSQ Z-source [23]	(D+2)/(1-D)	(G+1)/3	-	5	-	2	6
SL-Boost [18]	(D+1)/(1-D)	G	G	1	4	2	1
SC-Boost [18]	2/(1-D)	G/2	G/2	1	3	2	1
APICs-based [11]	(5D+1)/(1-D)	(2+G)/3	1+G	3	11	6	1

PV F + PrD = PD (36)

As seen in (37), the ESR and current of the inductor are related to its losses.

$$P_{rL}=r_L I^2 \quad (37)$$

To determine the power losses in the output capacitor, the current of Co is required. The value of (38) determines this current.

Consequently, the following relation is used to compute the capacitor's power losses.

rCI2 = PrC (39)

The total power losses are derived from (40). Ploss is equal to

TABLE:1COMPARISONBETWEENTHEPROPOSEDCONVERTERSANDOTHERSC/SL-BASEDSTEP-UPSTRUCTURES

Pd + PD + PrL + PrC (40)

Lastly, (41) is used to compute the efficiency.

With IGBT switches, ISH-SL-SC's efficiency is replaced in (42) by voltage gain. For MOSFET switches, the identical computation is done with (43) in mind. To circumvent complex equations, we substitute alternative letters in equations (44) through (53).

$$1 \quad \frac{1}{A1+B1+C+1} \tag{42}$$

$$\frac{1}{2} = A2 + B2 + C + 1 \tag{43}$$

$$A1 = \frac{V_{CE-} \quad (5G+1)(4\ \overline{D1}+\overline{D2})}{8GV0} \tag{44}$$

$$A2 = \frac{\frac{9}{64} r_{oni}\,(8D1+D2)}{R0} \tag{45}$$

$$B1 = \frac{3}{9}\,(E_{on+E_{off}})\,fs \tag{46}$$

$$B2 = \frac{0}{2G^2} \tag{47}$$

$$C = \frac{V_{FW}}{4V0} + \frac{1B\,ri+1c\ \ (h+m)}{R_0} \tag{48}$$

$$m = (G+1)(\overline{D1^{+D}2} + 1\overline{-D\_D-2} \tag{49}$$

$$j = G^{2+\ 10G+25} \tag{50}$$

$$\mathrm{u} = G^2 + 6G + 9 \tag{51}$$

$$n = D_{1\,(G^2+6G+8)+D_{2\ (G^2\ +\ 6G+25)+2}} \tag{52}$$

$$h = (D_{1+D_{2)(15-G^{2-2G})+G^{2+2G+1}}} \tag{53}$$

VI. A COMPARISON OF PERFORMANCE

Table I is provided to assess a thorough performance comparison between the suggested structures and earlier models. The voltage gain, maximum voltage stress across the semiconductors, and component count of these architectures are compared.

As stated in Section II, the addition of the auxiliary switch S3 in this work enhances the performance of the ANC [19] converters. Other research in this area, including [1], [11], [14], [15], [18], and [23], In order to give significant voltage gains, [25] created comparable non-coupled and non-isolated structures that integrated the fundamental sub-structures ASL, PSL, and SC as hybrid structures. Table I shows that the suggested structures' voltage improvements rely on both duty cycles D1 and D2. As you can see from Table I's second column, D2 really plays the part of the modifier to attain a big gain. On the other hand, one duty cycle governs other structures. It is important to remember that a constant D2 can help to simplify the control function of switches be put to use. Consequently, because D1 can provide a wide range of voltage gains, applying constant D2 results in no malfunction.

This figure shows that the suggested structure has a moderate slope for D2=30% and can produce a larger voltage gain than alternative designs for a variety of duty cycles. Furthermore, large duty cycles are not necessary for the ISH-SL-SC converter to produce significant voltage gain.

Figs. 6(a) and 6(b) show comparisons of the voltage stresses of semiconductor devices. For example, the maximum voltage stress of switches and diodes is computed in the same voltage gain (G=5) for all designs described in Table I in order to explain the good performance of the proposed structures. The findings indicate that in ISH-SL-SC, the primary switches' voltage stress is equivalent to that of SC-ANC [14].

SL/SC-SBC [15], SC-SL-ANC [19]. It is, nonetheless, smaller than the voltage stresses of other structures that function well. Furthermore, the ISH-SL-SC structure exhibits lower voltage stress than other structures when compared to the voltage stress across the diodes. It follows that the suggested architectures should function correctly in terms of the voltage stress across the semiconductor devices. It is evident that, in contrast to the IAH-SL and ISH-SL converters, the ISH-SL-SC converter has a lower voltage stress on the auxiliary switch in addition to its high voltage gain. The addition of SC cell is the cause of this decline. Actually, the auxiliary switch and the SC cell's diodes share the voltage stress of Vo. The total of (21)and (24)

$$V_{s3}^{stress} + V_{D4a,D4b,D4c}^{stress} = V_O \qquad (54)$$

Fig. 7 compares the normalized average current of semiconductors vs voltage gain for CCM in terms of current stress. Fig. 7(a) shows that, in contrast to the traditional topologies [5], [19], the average current rate in the primary switches stays lower for greater voltage increases. This comparison is also found for the diodes' maximum current in Fig. 7(b). Therefore, by reducing conduction losses, the efficiency of the suggested structures is increased. Table I compares the quantity of switches, diodes, inductors, and capacitors among other components. This table indicates that, among the structures that are constituted, HSXSQ Z-

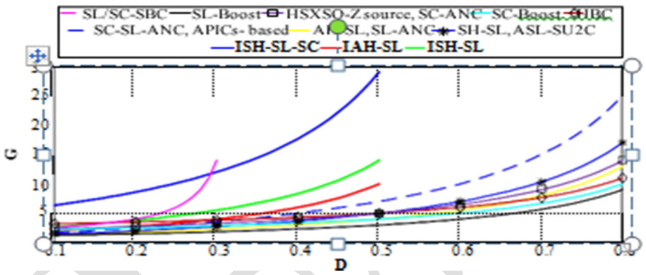

Figure 5 shows a comparison of the suggested converters' voltage gains with those of other converters.

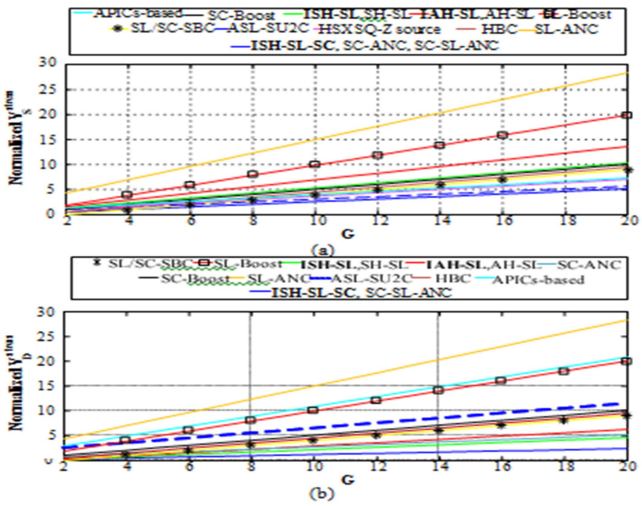

Figure 6 shows a comparison of the suggested converters with alternative converters. (a) Switch normalized voltage stress. (b) The diode's normalized voltage stress.

The source with the most number of swaps is [23]. The suggested structures also occupy the following rank. Still, the change in the quantity of switches is the addition of the auxiliary switch. In actuality, benefits like increased voltage gains and efficiency result from even a minimal adjustment in the number of switches.

Furthermore, compared to the ISH-SL-SC converter, [11] has a comparatively larger number of diodes and inductors. Lastly, in contrast to other architectures, we do not use a lot of capacitors.

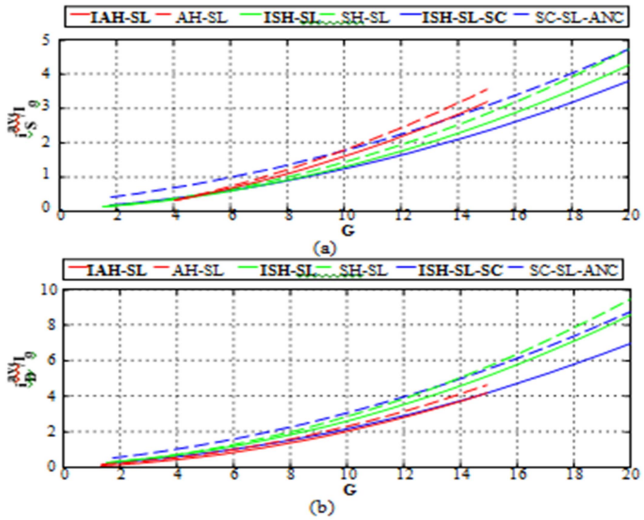

Figure 7 shows a comparison between the suggested enhanced converters and the standard converters. (a) Switch average current normalized. (c) The diode's normalized average current.

VII. EXPERIMENTAL ANALYSES AND SIMULATIONS

A. Describe the experimental configuration

This subsection describes the low input voltage application-specific design features of a prototype ISH-SL-SC. As per (13), the value of Vo is 78 V for Vin=3 V, D1=50%, and D2=30%. Furthermore, as mentioned in (14), the minimal value of inductors L1a, L1b, L2a, and L2b in the HSSL sub-structure is 345 µH for ΔiL=25% and fs=20 kHz. Additionally, (28) states that the value of Cmin for ΔVCo=25% is 696 µF.

A laboratory prototype of the suggested construction is put into practice for experimental validation based on the aforementioned parameters. During the practical test, fast IGBTs withAs semiconductor switches, high voltage and current ratings are employed. Switching pulses are produced via the ARM-based digital control platform ARDINO DUE R3. Through buffers and an optocoupler, this pulse generator is coupled to the gate driver of the IGBT. The two stacked boards that make up the implemented converter are seen in Fig. 8.

Three IGBTs, two DC voltage sources, three gate drivers, and constant values of D1=50%, D2=30%, and fs=20 kHz are utilized. The LCR test of all inductors reveals that the resistance rL and inductance L are 350 µH and 1.9 Ω, respectively. Three DC-DC converters housed in a compact SIP container are utilized to isolate the grounds. As a result, Table II provides a condensed summary of the parts that make up the prototype construction.

Fig. 9 displays the gate pulses that were generated for the switches. As a result, after turning off the S1, S2, and auxiliary switches, the S3 switch is switched on right away. After (D1 + D2)Ts, all switches are also switched off. Consequently Each switching period's switches turn on and off to complete one of the ISH-SL-SC's three operating modes.

B. Outcomes of the prototype and simulated ISH-SL-SC

A thorough simulation conducted in PSCAD/EMTDC has been conducted to validate the theoretical analyses. Moreover, an experimental prototype of the 100 W ISH-SL-SC is used to evaluate the operation modes. Figs. 10 to 14 show the steady-state outcomes of the suggested structure using the open-loop control approach. Figure 10 displays the experimental currents passing through SLs and compares them with the outcomes of the simulation. In Modes 1 and 2, these inductors get a charge from the input voltage Vin = 3 V, and in Mode 3, they transmit the necessary power to Ro.

Therefore, both the experimental and modeling findings show that the current of SLs has a trapezoidal wave form. The varying charging circumstances in Modes 1&2 (refer to Figs. 2a and 2b) result in variations in the charging slope of the currents of SLs, namely iL1a, iL2a, iL1b, and iL2b. These inductors have a peak to peak current ripple value of less than 0.5 A and a current ripple percentage of aroundΔiL equals 25%iL. As a result, it is seen that the experimental and simulated waveforms concur with the Section V theoretical operation analysis.

Figs. 12 and 13 give the necessary waveforms to examine the operating modes of switches and diodes. According to Fig. 12, the switches S1, S2 in the HSSL sub-structure have a maximum voltage stress of around 20 V, which is in line with the theoretical estimate of (15). Meanwhile, as shown in Fig. 12, the voltage of these semiconductor switches in Mode 2 is equal to Vin (3 V). Additionally, as seen in (21) the maximum voltage stress of S3 is half of the Vo (40 V). Figure 11 displays the voltage of the diodes D1a, D2a, D1b, D2b, D1c, and D2c in order to verify the intended operation of the HSSL sub-structure.

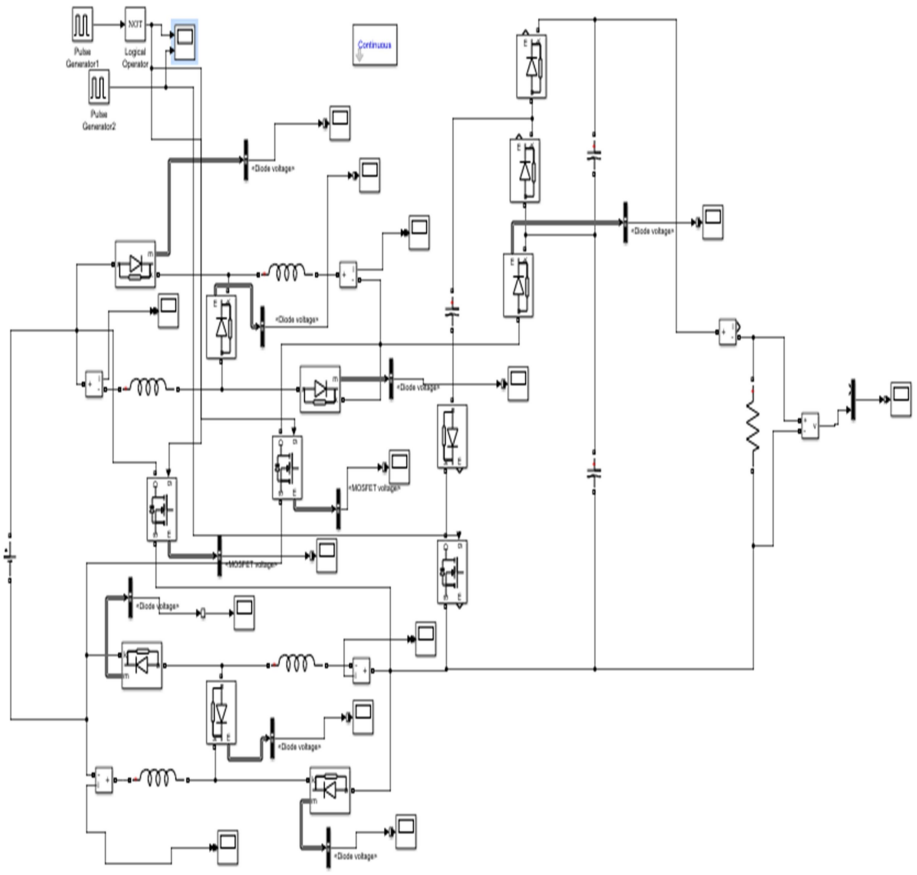

Fig 8: simulink diagram

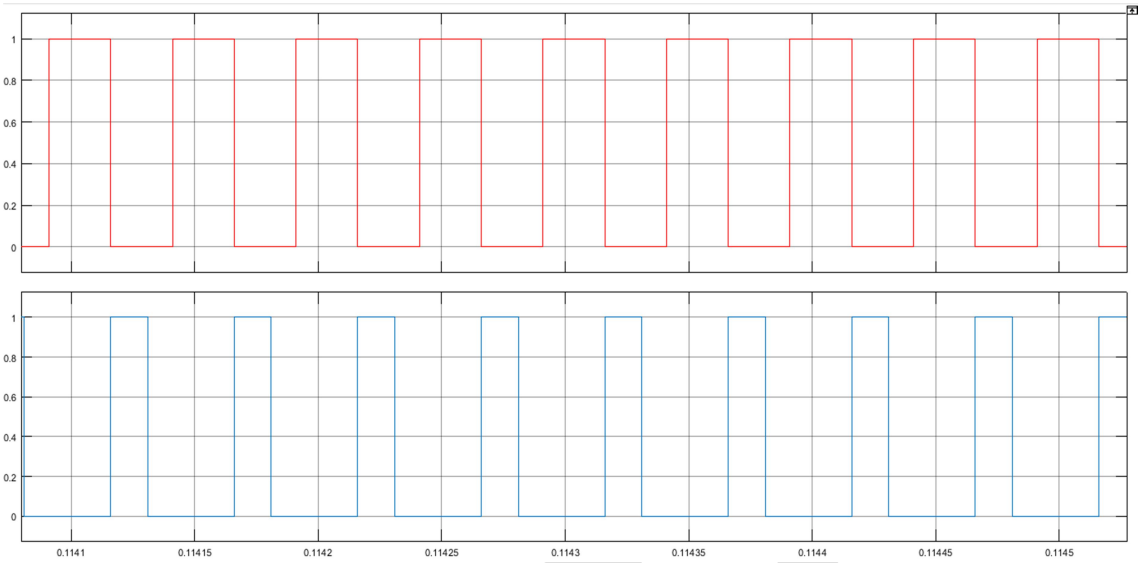

Fig. 9. Gate signals of S1, S2 and S3.

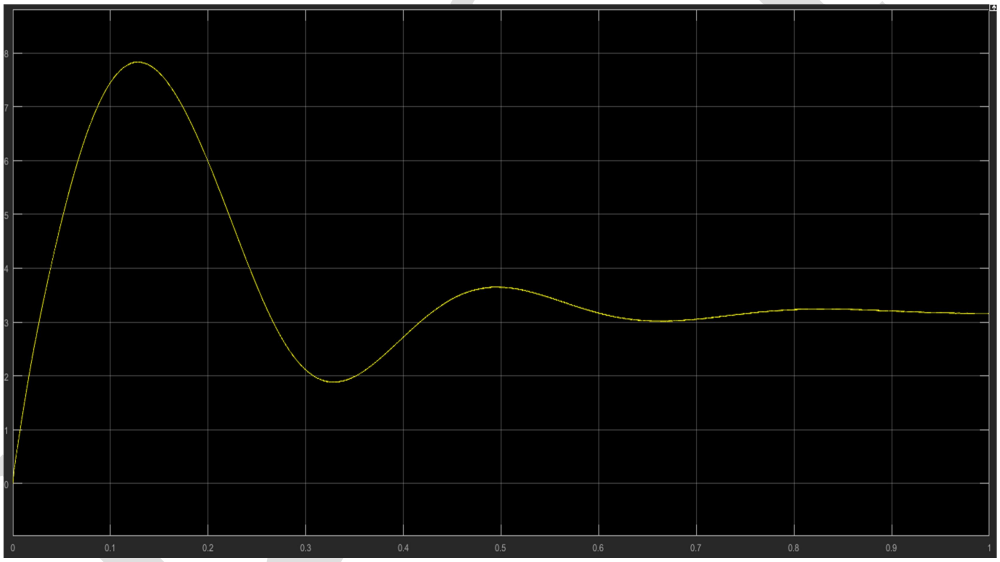

Fig. 10.Simulation current of the inductors.

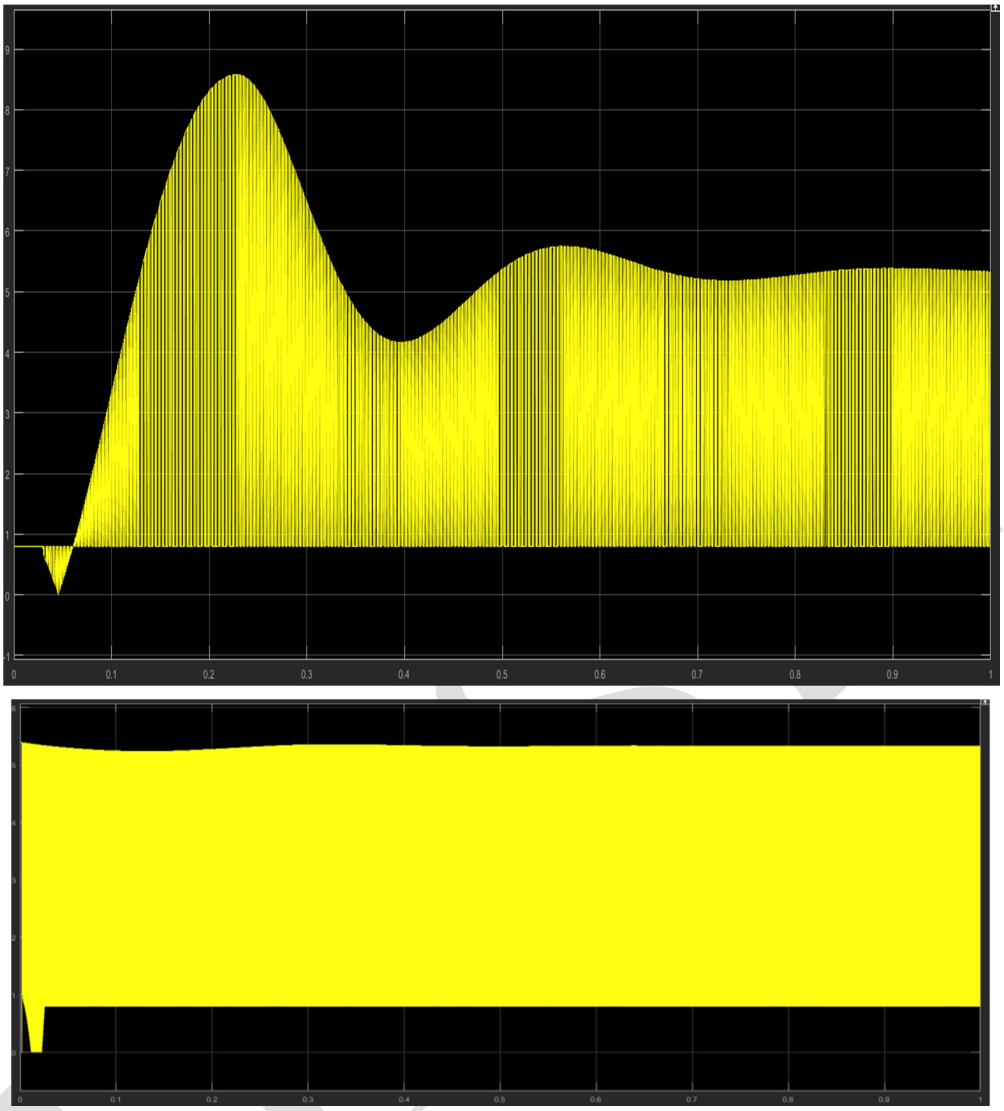

Fig. 11. Simulation waveforms of the voltages across the HSSL diodes

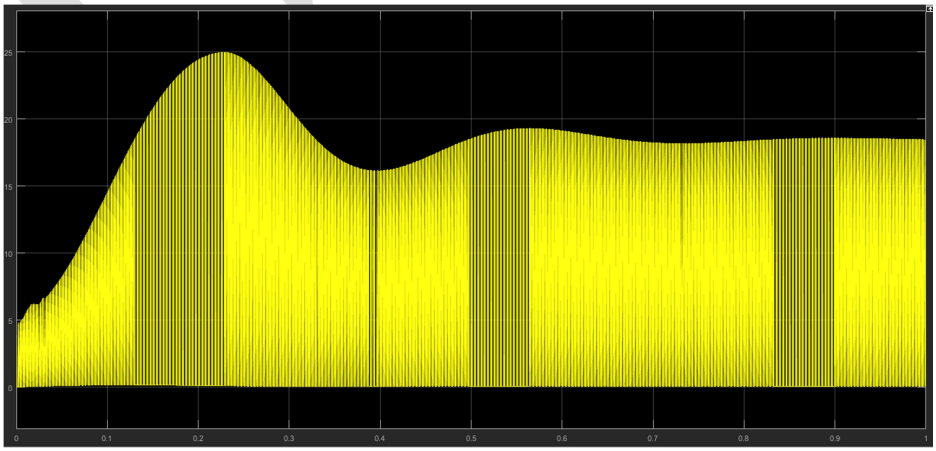

Fig. 12.Simulation waveforms of voltages across the switches

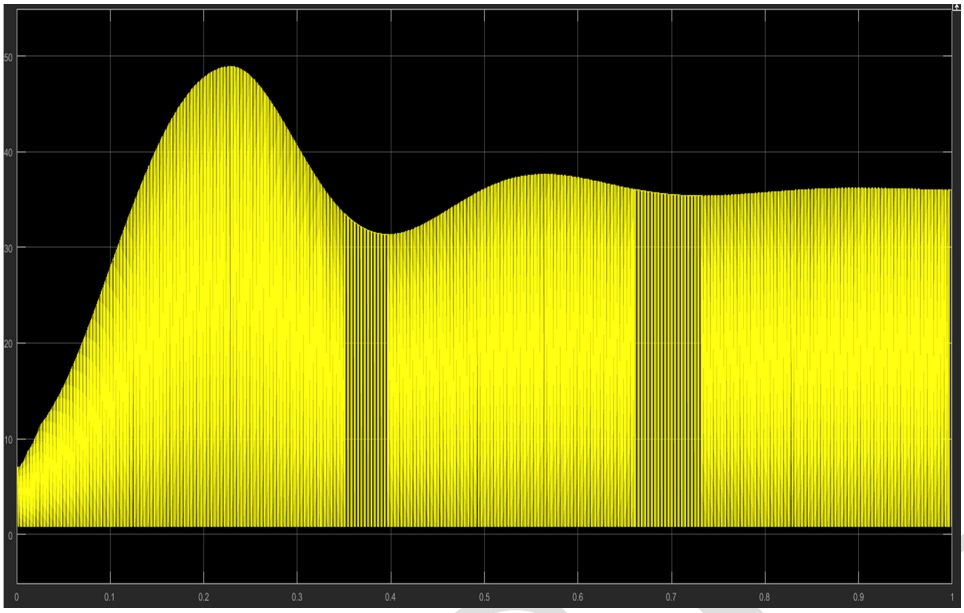

Fig. 13.Simulation waveforms of voltages across the SC diodes.

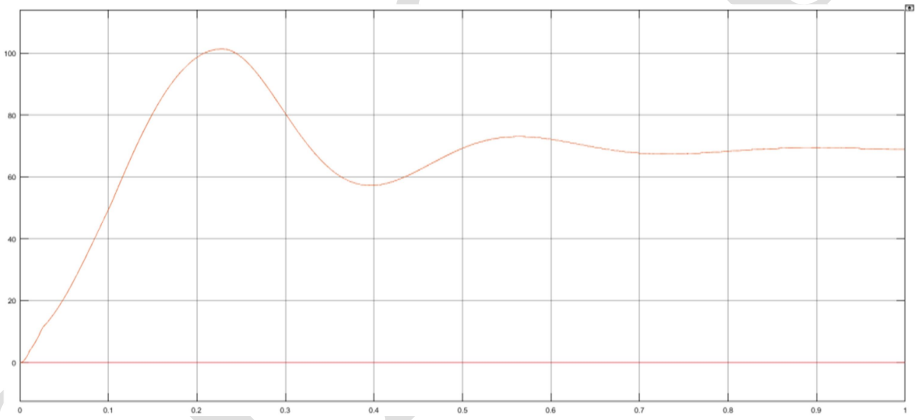

Fig. 14.Simulation waveforms of output voltage.

VIII. SUMMARY

This work presents a better construction of three non-isolated hybrid switched in- ductor/switched capacitor DC-DC converters. One may obtain the suggested converters by combining an auxiliary switch, PSL, ASL, and SC cells. These designs have the advantages of traditional converters with the potential to increase efficiency and voltage gain. As a result, the practical voltage gain exceeded 30 while the efficiency was improved by over 17%. We determined the appropriate sizes for inductors and capacitors as well as the precise voltage and current stresses of all the components. Moreover, parasitic components were added to the suggested converters to increase their efficiency. We used a variety of simulations and practical studies with an open-loop controller on our prototype to verify the veracity of our theoretical assessments.

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