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An Ultra-Low Leakage and Wide-Range Voltage Level Shifter for Low-Power Digital CMOS VLSI's

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ABSTRACT

This brief presents an ultra-low leakage and fast conversion level shifter with widerange voltage conversion and frequency. The proposed level shifter adopts the Transmission gate transistors, which can completely cut off the static current when the circuits stand by. The proposed level shifter also solves the swing problem and achieves a fast conversion, strengthening the pull-up network to ensure the internal node is fast and fully charged. Measurement results based on the 45 nm Cadence tool show that the average ultra-low leakage of the proposed level shifter is 34.8 W when converting from 0.4 V input to 1.08 V output. Meanwhile, the average propagation delay and the average energy per transition of the proposed level shifter are Low.

1-INTRODUCTION

The increasing demand for portable electronic devices, such as smartphones, wearables, and IoT devices, has led to a growing need for energy-efficient digital circuits. One of the most effective ways to reduce power consumption in these devices is by lowering the supply voltage. However, reducing the supply voltage also decreases the operating speed and affects the performance of the system.

To address this, modern digital circuits use multi-voltage domains, where different parts of a system operate at different voltage levels to optimize power and performance. In such multi-voltage systems, voltage level shifters (LS) play a crucial role in ensuring proper communication between circuit blocks operating at different voltage levels.

A level shifter converts low-voltage signals from a lower power domain to a higher voltage domain (or vice versa), enabling seamless operation across the system.

Importance of Voltage Level Shifters in Low-Power Circuits:

Voltage level shifters are essential in System-on-Chip (SoC) designs, where different functional units may have different supply voltage requirements. Some critical applications include:

- Microprocessors and SoCs: Multiple voltage domains for power optimization.
- IoT Devices & Wearables: Ultra-low power operation for extended battery life.
- Wireless Sensor Networks (WSN): Energy-efficient data transmission.
- Memory Interfaces: Voltage translation between different logic families.

Static Power Consumption:

- Many LS circuits suffer from static leakage currents, especially in deep submicron CMOS processes.
- Conventional differential cascade voltage switch-based LS (DCVSLS) circuits exhibit significant static power due to contention between pull-up and pull-down networks.

High Propagation Delay:

- Some LS designs experience slow transitions, especially when converting from very low voltages (e.g., 0.3V to 1.2V).
- Weak pull-down networks in sub-threshold regions lead to reduced switching speed.

Swing Reduction Problem:

- In some designs, the output voltage swing is not fully achieved, leading to incomplete logic transitions.
- This problem results in increased power dissipation in subsequent stages.

Process, Voltage, and Temperature (PVT) Variations

- CMOS circuits exhibit performance variations due to fabrication inconsistencies and environmental changes.
- LS designs must be robust across a wide range of PVT conditions to ensure reliable operation.

2-LITERATURE SURVEY

Level shifters are crucial circuits in modern mixed-voltage systems, enabling reliable communication between different voltage domains. As the demand for low-power and high-performance integrated circuits increases, especially in applications like IoT, mobile, and biomedical devices, the importance of efficient level shifter designs has grown significantly. Among various level shifter topologies, Transmission Gate (TG) based level shifters have received considerable attention due to their relatively simple structure, bidirectional signal transmission capability, and compatibility with CMOS technology.

Transmission gate level shifters operate by exploiting the bidirectional nature of transmission gates to pass logic levels from a low-voltage domain to a higher one (or vice versa). These designs often demonstrate low delay and moderate power consumption, making them suitable for moderate-speed and low-power applications. However, challenges such as leakage current, static power dissipation, and inability to operate reliably at ultra-low voltages (especially when the supply voltage difference is large) have motivated ongoing research into improved TG-based designs.

This literature survey aims to review the evolution of transmission gate-based level shifters, comparing various design methodologies, performance trade-offs, and innovations introduced to enhance robustness, reduce leakage, and improve energy efficiency. The survey also highlights recent advances addressing these limitations, including hybrid designs, body biasing techniques, and integration with hysteresis or keeper circuits.

Ultra-low power VLSI circuit design:

ULTRA-LOW power VLSI circuits are gaining considerable interest from the scientific community and more recently the market. Indeed, many recent and prospective applications explicitly rely on the availability of sensor nodes that are energy autonomous

and extremely small sized. A few examples of such applications are wireless sensor networks, biomedical and implantable devices/networks, ambient intelligence, wearable computing, smart grids, pollution monitoring, plant monitoring, smart warehouses. In the context of these applications and the related technologies, the main drivers are lifetime and size. Battery lifetime in the order of several years or decades would be highly desirable, although currently it is hardly within reach.

Millimeter size or less is also a target for future nodes, and some prototype is now available. Both lifetime and size are tightly constrained by the energy storage/scavenging device (they typically set the size of the whole node) and the node consumption. Since the battery technology has evolved much slower than CMOS technology, a considerable research effort has been devoted in aggressively reducing the

consumption of nodes, which today can be well below the micro watt for the above applications. Innovation will be constantly required to continue the historical 10–100 reduction in computers' size every ten years according to the Bell's law, while ensuring energy-autonomous operation.

A robust, high-speed and energy-efficient ultra-low voltage level shifter: STATE-OF-THE-ART system-on-chip (SoC) designs consist of several heterogeneous intellectual property (IP) blocks, each operating at a different supply voltage level depending on timing requirements. Time-critical blocks run at higher supply voltage (VDDH) to reach the target performance, whereas noncritical blocks operate at lower supply voltage (VDDL), even in sub-threshold regime, to save energy. Reliable level shifter circuits are required in such multiple VDD systems for a proper interfacing between different voltage domains, while maintaining the overall robustness of the design. Level shifters in prior art can be categorized to cross coupled (CC) and current mirror (CM) based topologies. Due to the presence of complementary pull-up networks (PUNs) and pull-down networks (PDNs), CC-based level shifters feature very low standby power consumption. As a drawback, they suffer from the current contention between the PUNs and PDNs during the switching, which affects both speed and energy. Such an effect is exacerbated when sub-threshold voltages need to be up-converted, requiring an impractical increase in size of the PDNs. Conversely, the CM-based architectures benefit from relaxed contention between PUNs and PDNs to improve speed and energy when a wide range up-conversion (i.e., from deep sub-threshold regime to a significantly higher voltage level) is required. Nevertheless, they typically suffer from large static power consumption. Different solutions were recently proposed in literature to overcome the above limitations of CC and CM based topologies. For example, adaptive/regulated PUNs are proposed to reduce current contention in CC-based designs, thus improving the switching speed and energy for up-conversions from extremely low-voltage domains. In addition, a split-input inverting buffer is used as output stage to further improve energy efficiency. In order to address the voltage drop and non-optimal feedback limitations of conventional CM-based level shifters, a revised Wilson CM exploiting mixed-threshold voltage (VTH) devices is proposed. A reduced-swing output buffer design allows lowering standby power, while a pass transistor-based circuitry improves the switching speed. Instead, a self-controlled current limiter scheme is explored to realize voltage shifting from deep sub-threshold to above-threshold domains while improving delay, energy, and static power consumption. The split-input inverting buffer is also adopted in CM-based topologies to reduce the static current in the output stage.

An ultra-low voltage level shifter based on a self-biased low-voltage cascode CM scheme and a split-input inverting output buffer is introduced.

To the best of the authors' knowledge, this is the first work where such CM topology is proposed and validated through silicon measurements for level shifter design. Moreover, the use of an additional diode-connected NMOS device along with a PDN boosting device in the driving scheme of the split-input inverting output buffer allows high energy efficiency, while ensuring fast switching.

3-INTRODUCTION TO EDA TOOLS

Electronic design automation (EDA) is the category

of tools for designing and producing electronic systems. This is known as ECAD (electronic computer-aided design) or just CAD. The objective of the project is to learn the design flow of System and Packaging level EDA tools, and to validate the tools for proper functioning.

The Cadence tool SCM (System Connectivity Manager) is used as an industry standard for System Level designing, Design Entry HDL organizes schematic information into and Cadence PCB Designer provides a scalable, full-featured PCB design solution. The validation is achieved using generation of test cases, based on either the company's own combination of design steps or based on the CCRs (Cadence Change Requests) filed by the leading customers which are confidential, since the end product based on the design issues is still to be launched in the market.

The verification based on these issues not only enhances the validation skills, but also provides an insight into the level of complexity at which the System Level Design companies like QUALCOMM, ERICSSON, IBM, CISCO, HP etc work. Validating the tool not only hones the testing/debugging skills but also greatly improves the design concepts both in the hardware and the software domains. The tools are designed and validated for different platforms viz. Linux, Solaris, Windows XP etc.

The scripting language Tcl are used for making the test case generation and automation tasks more efficient with respect to time consumption. In this report significant weightage has been given to understand the design flows of the Cadence SCM, Cadence Design Entry HDL and Cadence PCB Designer based on the company's confidential user guides and design workshops.

EDA Technology:

Electronic design automation (EDA) is the category of tools for designing and producing electronic systems ranging from printed circuit boards (PCBs) to integrated circuits. This is sometimes referred to as ECAD (electronic computer-aided design) or just CAD. (Printed circuit boards and wire wrap both contain specialized discussions of the EDA used for those.). The tools work together in a design flow that chip designers use to design and analyze entire semiconductor chips.

The objective of the project is to learn the design flow of System and Packaging level EDA tools, and to validate the tools for proper functioning. Allegro Design Workbench (ADW) represents a suite of products that help implement collaborative design environment involving your design teams, methodologies, corporate design databases, and tools. In addition, you can use design lifecycle, library development and management, and data management features to control the design and library management processes.

Overview of EDA Tools and Technology:

Electronic Design Automation is using the computer to design layout, verify and simulate the performance of electronic circuits on a chip or printed circuit board. While the public

mostly focuses on the end products and is only moderately aware of the chips and circuits inside. EDA for electronics has rapidly increased in importance with the continuous scaling of semiconductor technology. EDA tools are also used for programming design functionality into FPGAs.

About Cadence:

Cadence Design Systems is the world's largest supplier of EDA technologies and engineering services. Cadence helps its customers break through their challenges by providing a new generation of electronic design solutions that speed advanced IC and system designs to volume. The primary corporate product is software used to design chips and printed

circuit boards.

4-HYSTERESIS-CONTROLLED LOW-LEAKAGE LEVEL SHIFTER (HCLL-LS)

The scaling in size and addition of more functional densities on digital Integrated Circuits (ICs) have given ascends to large power consumption per unit area. Power consumption of IC is one of the prominent design constraints out of speed and area. Power consumptions in VLSI are includes static, dynamic and leakage power consumption. The dynamic power consumption is a resultant of switching of load capacitance when different voltages and dependent of frequency of operation.

The static power is because of direct short circuit path between VDD and ground. Leakage power is due to leakage current arise from substrate-injection and sub threshold regimes; hence enough attention can be laid on leakage power reduction. The Power consumption at system level can be reduced by scaling power supply voltage, but the problems like voltage swing, leakage currents, and insufficient noise margins would start to originate with the supply voltage scaling and speed or delay depends on circuit topology.

In view of portable and handheld devices the power consumption has turn into most significant design constraint for VLSI designers as the frequency or charging of battery back. The increase in power consumption and reliability problem also rises in addition to packaging cost.

Hysteresis-Controlled Low-Leakage Level Shifter (HCLL-LS) specific level shifter uses CMOS technology and incorporates voltage hysteresis and leakage shut-off techniques to improve performance

Operation of HCLL-LS:

To achieve the fast pull-down of N2 and reduce the transmission delay, a low-threshold transistor MN5 is used in this circuit to build a fast pull-down network. At the same time, the timely shutdown of the pull-up network should also be considered for energy saving. Here, the transistor MN3 is inserted to close the current mirror quickly once the internal node N2 is completely charged. When the input changes from low (VSS) to high (VDDL), as shown in. As the MN1 and MN2 are optimized with low-threshold transistors to strengthen the pull-down network, the MN1 and MN2 are turned on, and the current mirror charges the internal node N2 through the MP2 quickly.

However, when the input voltage of the conventional current mirror LS is near/sub- threshold, the pull-down network MN1 and MN2 are too weak to discharge the N1, which will decrease the current mirror charging time for the N2 and lead to the reduced swing problem which causes the high static current in the next stage buffer. To solve the problem, in this brief, a voltage hysteresis transistor MP3 is added to weaken the pull-up strength of MP1, the N1 maintains a lower voltage for the MP2 to have a faster speed to charge the node N2 fully, the current from MP2 to charge the node N2.

Meanwhile, the source of MN5 is equally connected to VDDL, which makes the MN5 completely cut off and prevents current leakage. this design could achieve a complete cut- off for the leakage current. With the employment of MP3, the reduced swing problem is significantly improved. Besides, to save energy, a leakage shut-off transistor MN3 is inserted, when the N2 is high, and the N3 changes to low, the MN3 is closed, and the current mirror is closed completely.

5- TRANSMISSION GATE LEVEL SHIFTER

A Transmission Gate Level Shifter is a type of voltage level translator used in CMOS- based digital circuits to interface two subsystems operating at different voltage domains. It plays a crucial role in modern low-power VLSI systems, especially when a

core circuit operates at a lower voltage (e.g., 0.4 V) and needs to interface with peripheral circuits at higher voltages (e.g., 1.8 V).

The Transmission Gate Level Shifter is a crucial circuit component used in modern VLSI systems to bridge logic blocks operating at different voltage domains. As technology scales down and power efficiency becomes a primary concern, designers often use low-voltage cores (e.g., 0.4 V) to reduce dynamic power, while peripheral or I/O circuits may still operate at higher voltages (e.g., 1.8 V). Direct communication between such blocks can lead to logic level incompatibility or even device damage. To solve this, a Transmission Gate Level Shifter facilitates safe and reliable voltage level translation, ensuring signal integrity across these domains.

Among the various types of level shifters, the Transmission Gate Level Shifter (TGLS) and the Hysteresis Controlled Low Leakage Level Shifter (HCLL-LS) serve different design objectives. It is designed for speed and full voltage swing, leveraging the bidirectional conduction of transmission gates to avoid threshold voltage drops. In contrast, the HCLL- LS is specifically tailored for ultra-low leakage applications, particularly in standby or near-threshold operation.

While TGLS offers faster operation and better signal fidelity in dynamic conditions due to its strong driving capability and full-swing output, it may suffer from higher leakage in sub-threshold regimes and lacks the ability to control transitions selectively. On the other

hand, HCLL-LS introduces controlled delay and hysteresis windows, which helps in minimizing leakage current, but often at the cost of speed and increased design complexity.

Design Considerations for TGLS:

- Ensure transmission gate transistors are sized properly to handle the load.
- Avoid signal degradation due to incomplete switching (e.g., under slow transitions or weak control signals).
- Use complementary gate signals derived from a control circuit that spans both voltage domains

Operation of Transmission gate Level Shifter (TGLS):

Transmission gate is the basic circuit element used in the transmission gate Level Shifter designs.

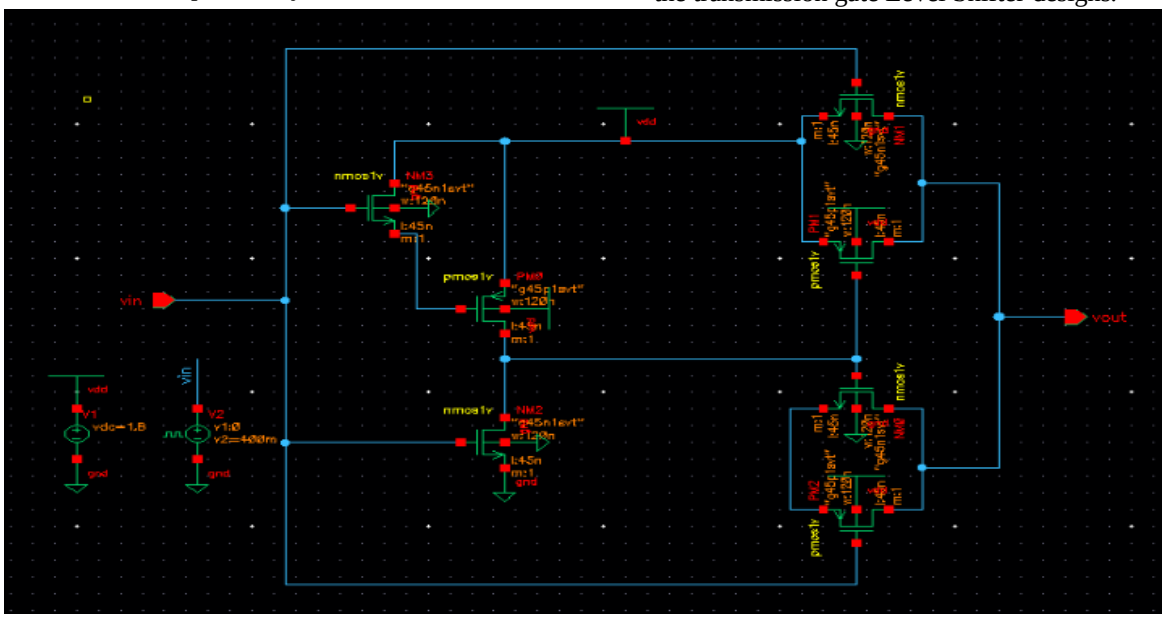

Fig 6.1: schematic of Transmission gate Level Shifter

It's ON resistance is less than the ON resistance of the NMOS, as ON resistance is low the lower transition times results in the output which reduces the delay and avoids contention mitigation.

The schematic provided illustrates a CMOS-based transmission gate level shifter. The circuit is composed of complementary MOS (NMOS and PMOS) transmission gates, cross-coupled inverters, and control logic. The input signal, denoted as vin, originates from the lower voltage domain and must be translated to a higher logic level, represented by vout. Two DC voltage sources are used: one at 0.4 V (low voltage) and another at 1.8 V (high voltage). The circuit employs both NMOS and PMOS transistors arranged in such a way that they form transmission gates-bidirectional switches capable of passing both logic high and low without significant signal degradation.

At the heart of the circuit lies a pair of cross-coupled inverters that form a positive feedback latch. This latch serves a critical role in restoring and holding the output to a strong logic level, either VDD (1.8 V) or GND. When vin is low (0 V or 0.4 V), the internal logic enables the pull-up path through a PMOS transistor while disabling the pull-down NMOS path. This causes one node in the cross-coupled inverter to rise to VDD, which in turn pulls the output vout to logic high. Conversely, when vin is high (0.45 V), the logic reverses the NMOS path is activated while the PMOS is disabled, pulling the output down to logic low (0 V).

The transmission gates ensure that this switching is efficient and that voltage levels are not degraded due to threshold drops, as might happen with single-transistor pass gates. The presence of both NMOS and PMOS transistors in the transmission gates is vital. NMOS transistors are efficient at passing logic low but struggle with logic high due to threshold voltage loss. PMOS transistors have the opposite characteristic. When used together in a transmission gate configuration, they compensate for each other's weaknesses, enabling full-swing logic levels to propagate through the gate regardless of the input voltage. This architecture ensures that the level shifter can reliably translate a 0.4 V signal to a full 1.8 V logic level without distortion or timing errors.

Overall, the transmission gate level shifter in the schematic offers several advantages, including low static power consumption, full-swing output, and high noise margin. Its structure ensures robust and fast level conversion suitable for systems where timing, area, and power efficiency are critical. This makes it especially useful in mixed-voltage SoC designs where reliable communication between low-voltage cores and higher-voltage peripherals is essential.

Table 6.1: Summary of Operation of TGLS

Input Voltage	**Transmission Gate Action**	**Output Voltage**
0 V (low)	Passes high to inverter	0 V (high domain logic 0)
VDDL (high)	Passes low to inverter	VDDH (high domain logic 1)

Simulation of TGLS:

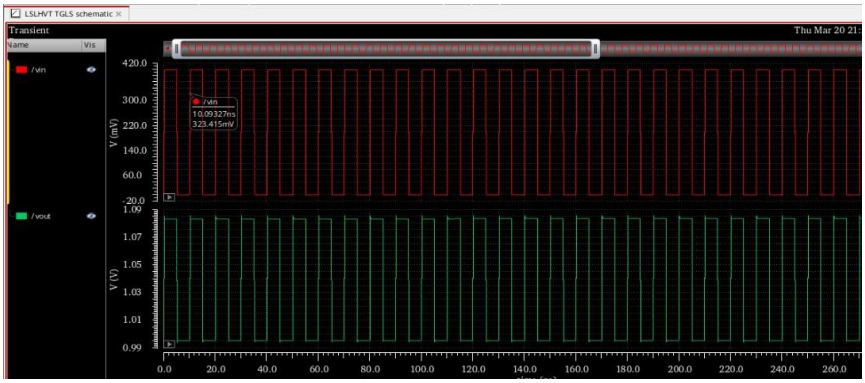

Fig 1: Simulation results of Transmission gate Level Shifter

The performance of the Transmission Gate Level Shifter (TGLS) was evaluated through transient simulation, power analysis, and physical layout extraction using a 45nm CMOS process. The transient response, as shown in the waveform, demonstrates the correct level shifting functionality where the input signal toggling between 0 V and 1.0 V is successfully translated to an output swing from 0 V to 1.8 V. The output waveform maintains full swing and clean transitions with minimal overshoot or ringing, indicating robust signal integrity.

The measured delay from the simulation shows that the output transitions lag behind the input by approximately 537.038 ps, indicating acceptable speed performance for level shifting applications.

The output voltage of the LS achieves a higher value, and its slew-rate is not affected. As the output node of TG Level shifting buffer resulting in less current being supplied to the output node. A higher output value of buffer and improved output slew rate provides the dynamic-energy efficiency and performance benefit due to current in the circuit does not need to pass for a longer time and there is no contention as well.

Power Analysis of TGLS:

Fig 2: Power analysis of Transmission gate Level Shifter

The power performance of the Transmission Gate Level Shifter (TGLS) was assessed through post-layout simulation using a 45nm CMOS process. The simulation setup involved applying a 1 MHz input

signal toggling between 0 V and 1.0 V, with the output shifting to a 0 V to 1.8 V range. From the transient waveform analysis, Static power consumption by the proposed method is 337.69 Nano watt. Dynamic power consumption by the proposed method is 972.52 Pico watts. And average power consumption is around

166.9 Nano watts. Transmission gate LS reduces the Dynamic and leakage power consumptions.

This value indicates a relatively low dynamic power dissipation, making the TGLS suitable for medium-power applications. The low dynamic power can be attributed to the minimal internal switching activity and the use of transmission gates, which reduce the need for static current paths.

However, transmission gates inherently involve both NMOS and PMOS transistors being active during switching transitions, which may cause slightly higher short-circuit current compared to conventional single-ended designs. Additionally, leakage power is present due to the constant gate biasing required for transmission gate operation, although it remains within tolerable limits for many digital systems.

Overall, the TGLS provides an efficient power profile with acceptable leakage and low dynamic consumption, striking a good balance between performance and energy efficiency. This makes it a practical choice for systems where high-speed level shifting is needed with moderate power constraints.

Layout of TGLS:

The physical layout of the TGLS was using Tanner EDA tool, and the area analysis was conducted using the Area Calculator tool. The layout occupies a total area of 49.5162 µm² with a maximum bounding box (MBB) of 15.82 µm × 18.87 µm, and a utilization density of approximately 16.587%. The layout maintains a clear and symmetric structure, which helps minimize mismatch between differential signals and eases routing congestion.

The layout is compliant with DRC rules, and parasitic extraction confirms that the design is capable of meeting the functional and performance criteria. The transmission gates and cross-coupled inverters were placed to optimize signal flow and reduce parasitic capacitance, thus enhancing speed performance.

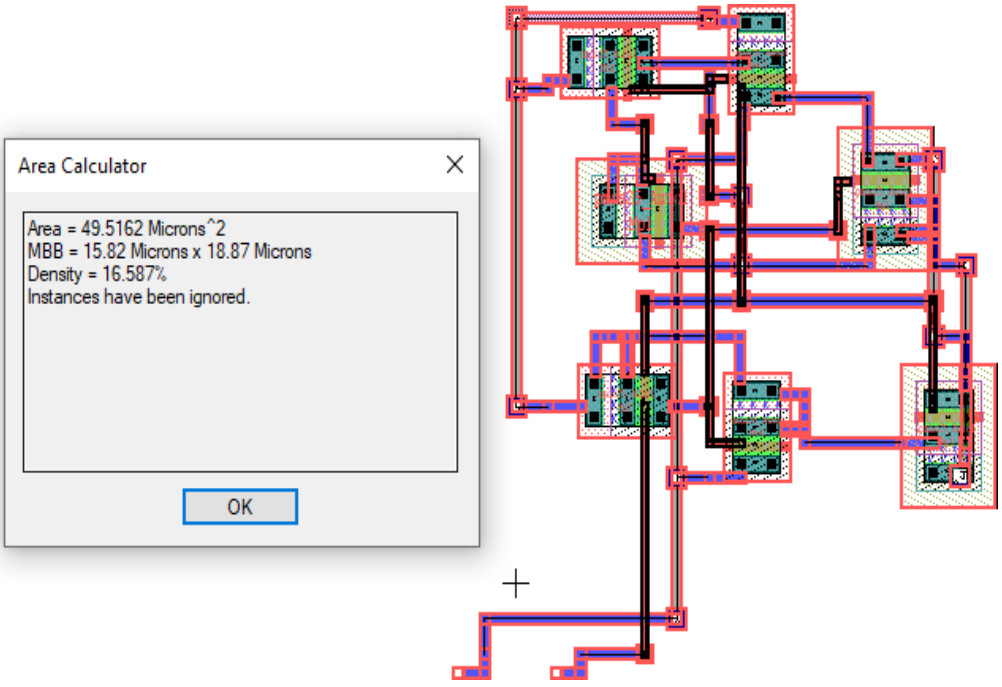

Fig 3: Layout of Transmission gate Level Shifter

In summary, the TGLS demonstrates strong advantages in terms of speed and compact layout compared to more complex designs like the Hysteresis Controlled Low Leakage Level Shifter (HCLL-LS). While the power consumption is slightly higher due to transmission gate leakage, the propagation delay is significantly reduced, making TGLS highly suitable for high-speed inter-domain voltage interfacing where leakage is not the dominant concern.

6-CONCLUSION

With the employment of the transmission gate transistors, which ensure fast charging to the internal node and solve the reduced swing problem and reduce the static power consumption and dynamic power consumption obviously, the proposed level shifter achieves fast voltage conversion and high energy efficiency.

The proposed design is fabricated in the 45 nm low-power process, a wide conversion ranges from 0.4 V to 1.08 V. The proposed level shifter shows high energy efficiency and significantly improves static power compared with the other State-of-the-Art level shifters.

The Transmission Gate Level Shifter (TGLS) offers an efficient and straightforward solution for voltage level translation in mixed-voltage digital systems. Through the use of complementary NMOS and PMOS transmission gates along with cross-coupled inverters, TGLS achieves full-swing output, low propagation delay, and compact layout, making it highly suitable for high-speed applications. Simulation results demonstrate successful level shifting from 1.0 V to 1.8 V, with low dynamic power consumption and acceptable leakage levels. Additionally, the layout implemented using Tanner EDA confirms the design's area efficiency and compliance with fabrication rules.

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