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Energy-Efficient Wide Range Level Shifter with a Logic Error Detection Circuit

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ABSTRACT

This project aims to create an energy-efficient, wide range level shifter (LS) with a logic error detection circuit (LEDC) is proposed. The proposed LS is designed based on a current mirror- based LS (CMLS), and a feedback pFET is added to solve the static current, which is a limitation of the CMLS. Similarly, Wilson's CMLS (WCMLS) solves the problem of the CMLS through the feedback pFET, however, it cannot convert low supply voltage (VDDL) to high supply voltage (VDDH) fully due to the feedback pFET. In contrast, the proposed LS can convert VDDL to full VDDH using the LEDC. To verify the performance between the proposed LS and the previously proposed LS, the post layout simulation was performed using the 32-nm finFET model.

1-INTRODUCTION

Lowering the supply voltage is an effective way of reducing the dynamic power consumption of the system-on-chip (SoC). This is because the dynamic power consumption of the SoC is proportional to the square of the supply voltage (VDD). Accordingly, operating a circuit in the near-threshold region can reduce the dynamic power consumption by almost ten times compared with the nominal supply voltage operation. However, with the use of the near-threshold VDD, degradation in the circuit operation speed is inevitable, making the circuit more vulnerable to noise. Thus, to achieve power efficiency while minimizing the negative effects on the speed and operation stability, it is desirable to use multi-VDD schemes; a high supply voltage (VDDH) is used for such noise-sensitive or speed-critical circuit blocks, while a low supply voltage (VDDL) is used for the remaining circuit blocks. When a multi-VDD is used, the signals from the blocks supplied with different voltages should not be directly connected. Instead, a level shifter (LS) that stably converts signals between different voltage domains is required. To utilize the wide range of VDDs in a single chip, the LS should be capable of converting the near-threshold voltage signal into the super threshold voltage so that the power efficiency can be maximized VDDH-powered pFET for positive feedback to start. Thus, when (VDDH–VDDL) increases, the contention is larger, causing functional failure. Hence, the voltage conversion range is limited, the CMLS, which is free from the contention problem. Even if VDDH–VDDL is large, the CMLS can convert VDDL– VDDH easily due to the diode-connected pFET. Thus, the CMLS has a wide range of input voltages than the CPLS. However, when IN is high after the transition, a large static current path exists (MP1–MN1), making it impractical because of the large energy consumption.

2-LITERATURE SURVEY

Ultra-low power VLSI circuit design demystified and explained

ULTRA-LOW power VLSI circuits are gaining considerable interest from the scientific community and more recently the market. Indeed, many recent and prospective applications explicitly rely on the

availability of sensor nodes that are energy autonomous and extremely small sized. A few examples of such applications are wireless sensor networks, biomedical and implantable devices/networks, ambient intelligence, wearable computing, smart grids, pollution monitoring, plant monitoring, smart warehouses. In the context of these applications and the related technologies, the main drivers are lifetime and size. Battery lifetime in the order of several years or decades would be highly desirable, although currently it is hardly within reach. Millimeter size or less is also a target for future nodes and some prototype is now available. Both lifetime and size are tightly constrained by the energy storage/scavenging device (they typically set the size of the whole node) and the node consumption. Since the battery technology has evolved much slower than CMOS technology, a considerable research effort has been devoted in aggressively reducing the consumption of nodes, which today can be well below the micro watt for the above applications. Innovation will be constantly required to continue the historical

10–100 reduction in computers' size every ten years according to the Bell's law, while ensuring energy-autonomous operation.

A high speed and energy-efficient ultra-low voltage level shifter

STATE-OF-THE-ART system-on-chip (SoC) designs consist of several heterogeneous intellectual property (IP) blocks, each operating at a different supply voltage level depending on timing requirements. Time-critical blocks run at higher supply voltage (VDDH) to reach the target performance, whereas noncritical blocks operate at lower supply voltage (VDDL), even in sub-threshold regime, to save energy. Reliable level shifter circuits are required in such multiple VDD systems for a proper interfacing between different of voltage domains, while maintaining the overall robustness of the design. Level shifters in prior art can be categorized to cross coupled (CC) and current

mirror (CM) based topologies. Due to the presence of complementary pull-up networks (PUNs) and pull-down networks (PDNs), CC-based level shifters feature very low standby power consumption. The CM-based architectures benefit from relaxed contention between PUNs and PDNs to improve speed and energy when a wide range up-conversion (i.e., from deep sub-threshold regime to a significantly higher voltage level) is required. Nevertheless, they typically suffer from large static power consumption. Adaptive/regulated PUNs are proposed to reduce current contention in CC-based designs, thus improving the switching speed and energy for up-conversions from extremely low-voltage domains. In addition, a split-input inverting buffer is used as output stage to further improve energy efficiency. In order to address the voltage drop and non-optimal feedback limitations of conventional CM-based level shifters, a revised Wilson CM exploiting mixed-threshold voltage (VTH) devices is proposed. The split- input inverting buffer is also adopted in CM-based topologies to reduce the static current in the output stage. In this brief, an ultra-low voltage level shifter based on a self-biased low-voltage cascode CM scheme and a split-input inverting output buffer is introduced Moreover, the use of an additional diode-connected NMOS device along with a PDN boosting device in the driving scheme of the split-input inverting output buffer allows high energy efficiency, while ensuring fast switching

A wide-range static current-free current mirror-based LS with logic error detection for near-threshold operation

LOWERING supply voltage (VDD) is a very effective way to reduce dynamic and static power

consumption in electronic systems. However, lowering VDD makes circuits slower and degrades the stability. Thus, many electronic systems adopt multiple VDD structure, in which timing critical parts or analogy circuits operate with high supply voltage (VDDH), whereas other noncritical parts are powered by low supply voltage (VDDL) to maximize energy efficiency. Conventionally, VDD used in multi-supply system is in the super-threshold region, that is, VDD values are sufficiently higher than the threshold voltage (Vth). The challenge of CPLS is that pull-down devices should overcome turned on pull-up latch powered by VDDH, which limits the conversion range. Although the current mirror LS (CMLS) is free from this problem, there is a large static short circuit current when IN is high, and thereby, a lot of energy is wasted. To resolve the problems of CPLS and CMLS, various LSs have been proposed]. Although

the limitations of CPLS and CMLS are resolved, these previously proposed LSs have their own problems. This article proposes a wide-range LS based on the CMLS. With the logic error detection circuit that controls the pull up path of CMLS, the proposed LS not only needs not to overcome VDDH powered latch but also free from the problems from that other previously proposed LSs suffer.

A wide-range level shifter using a modified Wilson current mirror hybrid buffer

DYNAMIC VOLTAGE SCALING (DVS) has been widely used in digital processing elements for reducing energy consumption, and aggressive voltage scaling has extended the voltage range into the sub threshold region. The ultra-low power consumption of sub threshold operations facilitates the development of crucial applications, such as ubiquitous sensors and miniature health-care devices. Near-threshold operations of processors and memories achieve the optimal energy consumption, whereas sub threshold operations further reduce power consumption, enabling the operations of autonomous sensor nodes that rely on energy scavenging. However, from a system perspective, sub threshold operations are limited to part of the digital processing elements. Other system components, such as the power management unit, radio, actuators, and sensors, have distinct constraints in the supply voltage, where sub-to supra threshold level conversion is usually unavoidable. General-purpose applications also require wide-range level shifters (LSs) if a system involves at least one aggressive DVS domain. Wide-range LSs receive ultra-low voltage signals and use the weak drive current of pull-down networks (PDNs). When input level is sub threshold, the conversion results of LSs are vulnerable and easily affected by process, voltage, and temperature variations. Therefore, several sub threshold LSs were proposed to solve this problem.. Although these LSs can convert a sub threshold voltage, critical problems occur when using them in general DVS applications. First, previous sub threshold LSs may exhibit timing issues when the input and output levels are close. Ultra-low-voltage (ULV) processors and memories usually support sub threshold and supra threshold operations for enabling energy and performance trade-offs. Both wide-range and close- range level conversion are required to achieve this flexibility. The term “full range” indicates that the minimal of operating voltage can be deep sub threshold, close to the minimal supply voltage of the digital circuits, and the maximal operating voltage is the

standard supply voltage defined in a transistor technology. In addition to the operating range, the delay, power consumption, and duty cycle of LSs were carefully considered. The energy efficiency of wide-range level conversion was examined. The low slew rate of sub threshold signals may lead to a long

transition period and consume high short- circuit power. To reduce this power consumption, robust sub threshold LSs require amendments with proper voltage assignment.

3-SOFTWARE REQUIREMENTS

LT spice Tool

LT spice is a powerful and versatile simulation tool widely used for the design and analysis of electronic circuits. Developed by Analog Devices, LT spice provides a robust platform for simulating both analog and digital circuits. Its primary use is in the design and verification of circuits before physical implementation, enabling engineers to test their designs under a variety of condition and refine them without incurring manufacturing costs.

This document provides a comprehensive introduction to LT spice, covering its features, advantages, and applications. It also includes a step-by-step guide to using the tool, from basic operations to advanced simulations, making it suitable for both beginners and experienced circuit designers.

Overview of LT spice

LT spice, originally developed by Liner Technology, is a SPICE-based (Simulation Program with Integrated Circuit Emphasis) simulator. It includes:

A highly efficient SPICE engine optimized for faster simulations. An integrated schematic capture tool for circuit design. An extensive library of components, including model for Linear Technology devices and generic components like resistors, capacitors, and transistors.

Importance of LT spice in Circuit Design

LT spice enable engineers to validate circuit design before physical implementation, saving time and cost associated with manufacturing errors.

Analysis of Complex System: Engineer can simulate and analyses large-scale circuit, including power supplies, communication system, and analog signal processing units.

Education Tool: LT spice is an excellent platform for teaching and learning circuit theory, offering hands-on experience in circuit behavior and analysis.

Versatility: It supports a wide range of applications, including transient analysis, AC analysis, noise analysis, and more.

Installing LT spices

To get started with LT spice, follow these steps:

1. Visit the Analog Devices LT spice webpage to download the installer
2. Run the installer and follow the on-screen instructions to complete the installation.
3. Open LT spice to access the main interface.

User Interface of LT spices

The LT spice interface consists of the following components:

Schematic Editor: This is the main workspace where circuit are drawn and configured. Components can be placed, wired, and configured easily using intuitive tools.

Simulation Control: The toolbar includes options for setting up and running simulations. User can define the type of analysis, such as transient, AC, or DC sweep.

Waveform Viewer: This module displays simulation results in graphical form, such as voltage and current waveforms.

Component Library: A searchable library allows quick access to standard components like resistors, capacitors, transistors, diodes, and integrated circuits.

EDA Tools

Electronic design automation (EDA) refers to a comprehensive range of tools utilized in the design and production of electronic system. The term used to refer to this is EDA, which stands for electronic computer-aided design, or simply CAD. The objective of the project is to learn the design flow of

System and Packaging level EDA tools, and to validate the tools for proper functioning. The Cadence tool SCM (System Connectivity Manager) is used as an industry standard for System Level designing, Design Entry HDL organizes schematic information into and Cadence PCB Designer provides a scalable, full-featured PCB design solution. The validation is achieved using generation of test cases, based on either the company's own combination of design steps or based on the CCRs (Cadence Change Requests) filed by the leading customers which are confidential, since the end product based on the design issues is still to be launched in the market. The verification based on these issues not only enhance the validation skills, but also provides an insight into the level of complexity at which the System Level Design companies like QUALCOMM, ERICSSON, IBM, CISCO, HP etc work. Validating the toll not only hones the testing/debugging skills but also greatly improves the design concepts both in the hardware and the software domains. The tools are designed and validated for different platform viz. Linux, Solaris, Window XP etc. The scripting language TCL are used for making the test case generation and automation tasks more efficient with respect to time consumption. In this report significant weightage has been given to understand the design flow of the Cadence SCM, Cadence Design Entry HDL and Cadence PCB Designer based on the company's confidential user guides and design workshops.

4-EXISTING METHOD

There are some existing methods. In this section, operation, and limitations of the previously proposed Level Shifters (LSs) are briefly introduced. The operation of various LSs and the sizing of each transistor varies.

We have used systems such as RCC pull-up network, CPLS with a current limiter, CPLS with an adaptive current limiter, Wilson's CMLS, Osaki's LS, Hosseini's and Lotfi's LS. These are all Level Shifters.

RCC Pull-Up Network

Operation:

RCC pull-up network uses a resistive-capacitive (RC) coupling method to drive the signal levels. The resistor provides the necessary pull-up strength, and the capacitor enhances the switching dynamic by reducing delay. This method is simple and widely used for basic level shifting.

CPLS with Current Limiter (Conventional Pass Transistor Level Shifter)

This design incorporates a pass transistor with a current limiter circuit to control the current flow during level shifting. It aims to reduce power consumption during transitions.

CPLS with Adaptive Current Limiter

In this variant, the current limiter is adaptive and adjusts based on load and operation conditions, improving efficiency during transitions. It enhances the conventional CPLS design by offering dynamic adaptability.

Proposed Method

Cross Coupled Level Shifter (CPLS)

In this section, the structure and operation proposed LSs are briefly introduced. A Cross Coupled Level Shifter is a circuit used to shift voltage levels between different logic families or power domains while maintaining signal integrity. A Cross Coupled Level Shifter using FinFET is a voltage level conversion circuit that leverages Fin Field-Effect Transistors (FinFETs) instead of traditional CMOS transistors to achieve better power efficiency, faster switching, and reduced leakage current.

Operation

The circuit typically consists of complementary FinFETs (n-FinFET and p-FinFET), similar to

CMOS. It translates signals from low voltage (e.g., 0.8V or 1V) to higher voltage (e.g., 1.8V or 3.3V). A cross-coupled structure of FinFETs ensures proper voltage shifting with minimal power dissipation. Some designs incorporate dual-gate

5-RESULTS AND DISCUSSIONS

Schematic Result of CPLS

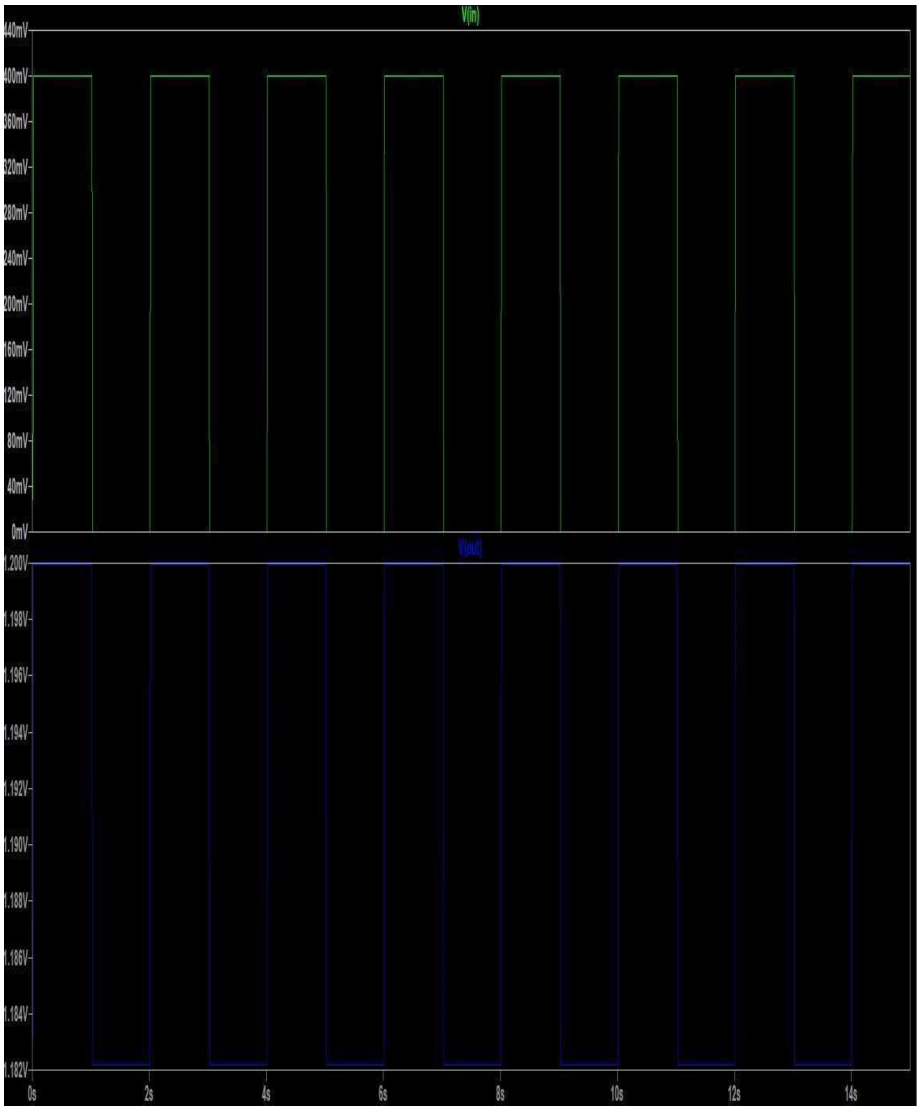

Fig 1 Simulation Result of CPLS

1. The top waveform (green) represents the low-voltage input signal (0 – 0.4 V).
2. The bottom waveform (blue) is the level-shifted output signal, correctly translated to the higher voltage level (0 – 1.8 V).
3. The output closely follows the input transitions, demonstrating proper level shifting and rail-to-rail output swing.
4. The output is clean, glitch-free, and shows minimal delay, indicating the circuit's suitability for real-time digital interfacing.

Layout of CPLS

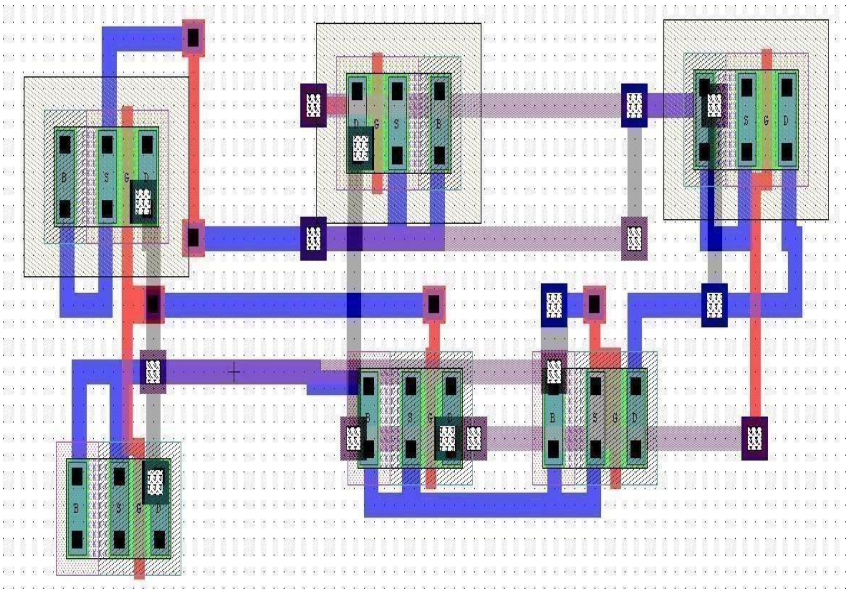

Fig 2 Layout and Area of CPLS

The layout shows the CPLS as shown in the figure represents a physical design implementation using Tanner EDA Tools with 32nm finFET Technology. This outlines the structure, operation, and limitations of previously proposed level shifters (LSs) using 32-nm FinFET technology, where transistor sizing is indicated by the number of fins and a fixed channel length of 20 nm. It highlights the regulated crosscoupled (RCC)

pull-up network-based LS, which incorporates diode-connected pFETs (MP3 and MP4) to mitigate contention issues. However, these pFETs limit the output voltage swing, reducing the conversion range and increasing output buffer power consumption. The accompanying CPLS schematic (Fig. 1.A) and its output illustrate an improved design approach,

likely aimed at achieving full-swing output and enhanced power efficiency compared to traditional LSs.

Simulation Result of CMLS

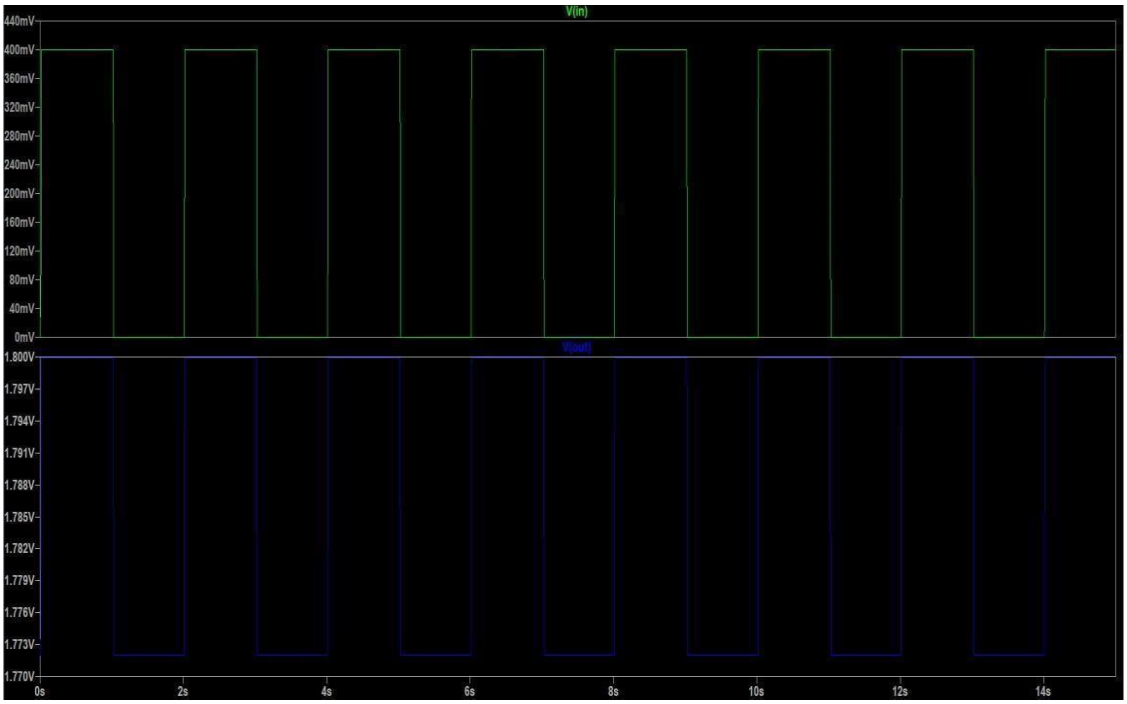

Fig 3 Simulation Result of CMLS

1. The graph shown is the transient simulation result of the level shifter, likely obtained from SPICE simulation (e.g., LTspice).
2. Green waveform (V(in)): Represents the input signal oscillating between 0V and 0.2V (low voltage domain).
3. Blue waveform (V(out)): Represents the output signal toggling between 0V and 1.8V (high voltage domain).

Layout of CPLS

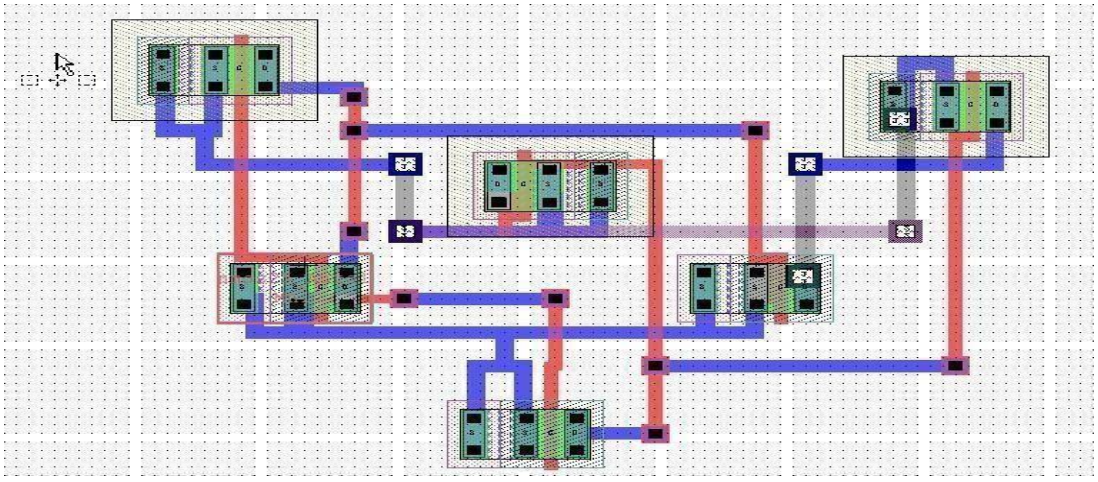

Fig 6.4 Layout and Area of CMLS

This layout shows how the components in the schematic (transistors, interconnects, and contacts) are physically arranged on silicon. The layout includes PFET and NFET transistors, represented by green and black diffusion regions. Metal layers (Red and Blue): Red typically indicates Metal 1, while Blue may indicate Metal 2, used for routing signals and power. Contacts and Vias connect different layers and transistor terminals (gate, source, and drain). Symmetrical structure indicates a balanced design, minimizing mismatch in the pull-up and pull-down networks.

6-CONCLUSION

In this brief, we propose an energy-efficient and wide-range LS that can convert a near- threshold voltage to a super threshold voltage by utilizing the current mirror structure. Due to the LEDC, the proposed LS only dissipates current in the transition state and solves the limitations of the WCMLS; thus, the proposed LS is capable of energy- efficient operation. Quantitative analysis was performed through a post layout simulation using the LTSPICE-32-nm model, which proved the superiority of the LS in delay and energy consumption

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