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Full Length Article

Adaptive DVFS(Dynamic Voltage And Frequency Scaling) Controller Using FSM In Verilog

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ABSTRACT
Power consumption has become a major concern in modern digital and embedded systems due to increasing performance demands and shrinking device sizes. Dynamic Voltage and Frequency Scaling (DVFS) is an effective low-power technique that reduces energy consumption by adjusting voltage and frequency according to system workload. However, conventional DVFS implementations rely on fixed operating modes and lack adaptive decision-making capability. This paper presents an Adaptive DVFS controller implemented using a Finite State Machine (FSM) in Verilog. In the first phase, a basic DVFS architecture is designed to demonstrate voltage and frequency scaling across multiple operating modes. In the second phase, an FSM-based adaptive control mechanism is introduced to dynamically select optimal voltage-frequency states based on workload conditions. The proposed design is modeled at the RTL level and verified through simulation using Vivado. Results demonstrate improved power-performance adaptability compared to traditional DVFS techniques, making the design suitable for low-power embedded and real-time applications.

Keywords : *Adaptive DVFS, Finite State Machine (FSM), Dynamic Voltage and Frequency Scaling, Low Power Design, Verilog HDL, RTL Design, Power Management, Embedded Systems.*

Introduction

Energy efficiency has become a major concern in the design of contemporary digital systems. The rapid expansion of mobile processors, embedded platforms, Internet of Things (IoT) devices, wearable electronics, and battery-powered systems has significantly increased the demand for computational performance. As performance requirements grow, power consumption, heat dissipation, and battery drain also increase. These issues directly affect system reliability, operating cost, and user experience. Consequently, reducing power usage while maintaining acceptable performance has become a key objective in modern VLSI and embedded system design.

Traditional low-power techniques such as clock gating and power gating are widely used to minimize unnecessary switching activity and leakage current. Although effective in specific conditions, these methods alone are insufficient for applications where workload demand changes continuously. Many real-world systems alternate rapidly between idle, moderate, and peak processing states. In such environments, static power-saving methods cannot provide the flexibility required for efficient runtime operation.

Dynamic Voltage and Frequency Scaling (DVFS) was introduced as a practical solution to this challenge. DVFS lowers processor clock frequency and supply voltage during periods of reduced activity, thereby decreasing dynamic power consumption. Since dynamic power is proportional to switching frequency and approximately proportional to the square of supply voltage, DVFS can achieve substantial energy savings. However, conventional DVFS implementations often depend on predefined operating states and software-based governors. These mechanisms usually respond at relatively slow intervals and are less effective when workloads fluctuate quickly.

Adaptive Dynamic Voltage and Frequency Scaling (ADVFS) extends the DVFS concept by introducing intelligent and workload-aware control. Instead of selecting from a small number of static operating points, ADVFS continuously evaluates system conditions and chooses the most efficient voltage–frequency combination in real time. Decisions may be based on processor utilization, queue depth, thermal conditions, performance demand, or predictive workload behaviour. This enables the system to deliver high performance when required while conserving energy during light workloads.

A critical challenge in implementing ADVFS is the safe coordination of voltage and frequency transitions. If frequency increases before voltage reaches a safe level, timing violations may occur. Similarly, lowering voltage before reducing frequency can compromise circuit stability. For this reason, deterministic control logic is essential. Hardware-based controllers using Finite State

Machines (FSMs) provide a reliable solution because they manage transitions according to predefined sequencing rules. During upward scaling, voltage is increased before frequency. During downward scaling, frequency is reduced before voltage. This structured behaviour improves stability and prevents unsafe operating conditions.

Hardware implementation also reduces transition latency when compared with software-driven approaches. Fast response is especially important in processors handling burst workloads, mobile applications, and real-time systems. By integrating clock-generation logic, synchronized switching circuits, and voltage control interfaces, ADVFS can operate smoothly with minimal delay.

In summary, ADVFS represents an advanced approach to intelligent power management. By combining real-time workload awareness, hardware-controlled decision making, and secure voltage–frequency coordination, it provides an efficient solution for next-generation low-power digital systems.

Methodology

The development of the Adaptive Dynamic Voltage and Frequency Scaling controller follows a structured hardware design methodology. The objective is to achieve reliable power optimization through deterministic control, safe operating transitions, and efficient performance adaptation. The proposed methodology is implemented using Verilog HDL and consists of several design stages.

Requirement Analysis and Parameter Definition

The first stage involves identifying system requirements and selecting the parameters required for adaptive scaling. These parameters include workload indicators such as processor utilization, task queue depth, or instruction activity. Operating modes are defined as Low-Power, Normal, and High-Performance states. Each mode is associated with a suitable voltage–frequency operating point. Additional constraints such as thermal limits, allowable transition time, and safe sequencing rules are also determined during this phase.

FSM-Based Control Design

The core controller is designed using a Finite State Machine. Each power mode is represented as a separate state, and transitions occur according to workload demand and system feedback. The FSM generates control signals for clock selection and voltage requests. It also enforces the fundamental safety rules: frequency must be reduced before voltage reduction, and voltage must be increased before frequency enhancement.

Multi-Clock Generation and Switching

To support different performance levels, multiple clock frequencies are generated using divider circuits or phase-locked loop resources depending on the target platform. Glitch-free clock multiplexing techniques are used to switch between clock domains. Synchronization circuits ensure stable operation during transitions and prevent metastability.

Designing Adaptive DVFS

The design of the ADVFS system focuses on developing a hardware-managed mechanism that adjusts processor performance according to real-time computational demand. The first step is to establish voltage–frequency operating points that satisfy timing and stability requirements. Typical modes include low-power operation for light workloads, normal mode for average activity, and turbo mode for intensive processing.

Once the operating points are defined, the FSM controller is implemented to manage transitions among these modes. The controller continuously monitors workload conditions and selects the appropriate state. If workload demand rises, the system first requests a higher supply voltage and then increases the operating frequency. If demand falls, frequency is lowered before voltage reduction. This sequence guarantees stable circuit timing.

A multi-clock subsystem is integrated to provide selectable frequencies for each mode. The switching network uses synchronized control signals and glitch-free multiplexers to ensure clean transitions. In addition, a voltage-request module communicates with the external regulator and confirms when the requested voltage level has stabilized.

The design also includes protection logic that checks for invalid transitions, unstable clocks, or unsafe thermal conditions. This safety layer ensures reliable operation under different runtime scenarios.

After implementation, extensive simulation is carried out using workload-driven testbenches. Waveforms are analyzed to verify correct state changes, clean clock transitions, and proper sequencing of voltage and frequency controls. Results are then compared with conventional DVFS systems to demonstrate improvements in responsiveness and energy efficiency.

Through this design methodology, the ADVFS controller achieves reduced power consumption, lower transition delay, and higher reliability, making it suitable for modern embedded and processor-based applications.

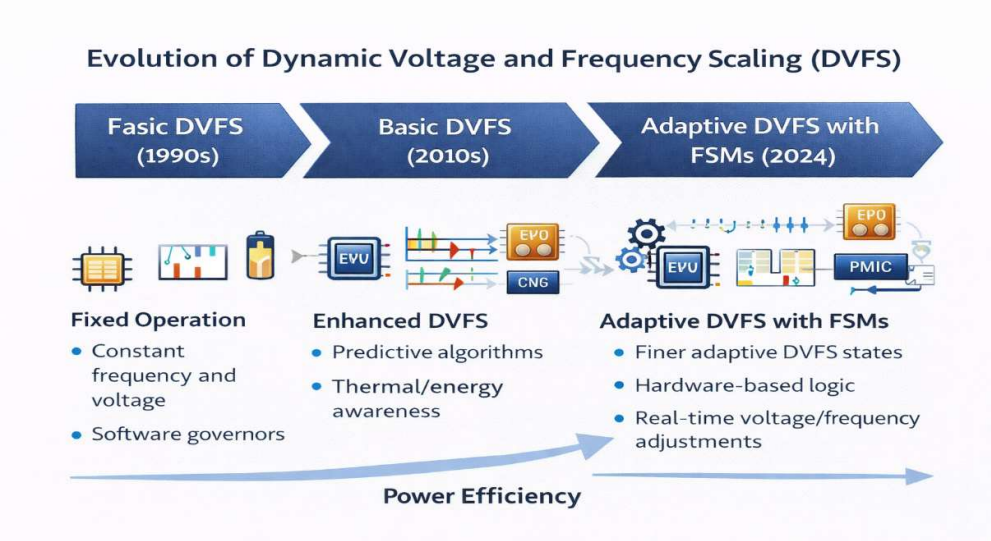

Figure 1; Evolution of the DVFS

LITERATURE SURVEY

Power management has become a fundamental concern in modern computing systems because of the rapid growth of portable electronics, embedded devices, and high-density VLSI circuits. As processing capability increased, energy consumption and heat generation also rose, creating a need for techniques that could lower power usage while maintaining acceptable system performance. Among the various approaches proposed in the literature, Dynamic Voltage and Frequency Scaling (DVFS) emerged as one of the most practical and widely adopted methods. DVFS reduces power consumption by adjusting processor supply voltage and clock frequency according to workload demand, thereby minimizing unnecessary energy expenditure during low-utilization periods.

Initial DVFS studies concentrated on simple operating-point selection, where processors switched between a limited number of predefined voltage–frequency states. These early methods demonstrated meaningful reductions in dynamic power consumption, but their control strategies were relatively inflexible. State transitions were often triggered through static rules or software-based governors, which were unable to respond efficiently to rapidly changing workloads. As applications became more interactive and multitasking environments became common, these limitations became increasingly visible.

Later research introduced more sophisticated DVFS frameworks that considered processor utilization, thermal conditions, and predictive workload behaviour. During the 2010s, several studies proposed adaptive policies that selected operating points using historical usage trends, analytical models, or feedback control mechanisms. Although these methods improved decision quality, many still depended on software layers for implementation. As a result, they suffered from response latency, scheduling overhead, and reduced suitability for time-sensitive systems.

To overcome these shortcomings, recent literature emphasizes hardware-assisted scaling mechanisms. In such systems, sensors, control logic, and dedicated controllers directly manage voltage and frequency transitions. Finite State Machine (FSM)-based architectures are particularly significant because they provide deterministic sequencing, low-latency transitions, and reliable timing control. These characteristics are essential in applications such as mobile processors, IoT nodes, and safety-critical embedded platforms.

The progression of published work therefore shows a clear transition from static DVFS methods toward intelligent, hardware-driven Adaptive Dynamic Voltage and Frequency Scaling (ADVFS). This evolution supports the need for advanced controllers capable of real-time adaptation while guaranteeing safe operating transitions.

Existing Methods

Several DVFS models have been introduced over time to improve processor energy efficiency. Each model contributed valuable insights, yet practical limitations remained. The most widely discussed methods include Static DVFS, Threshold-Based DVFS, Software-Governor DVFS, Predictive DVFS, Thermal-Aware DVFS, and Fine-Grained Multi-Level DVFS.

Static DVFS Model

Static DVFS represents the earliest generation of voltage and frequency scaling techniques. In this model, the processor operates using a small number of predefined performance states and changes state only when significant workload variation is detected. This approach offered better energy efficiency than running continuously at peak frequency. However, it lacked flexibility and could not react effectively to short-term workload fluctuations. Because of slow transitions and coarse

control granularity, systems either consumed unnecessary power or delivered insufficient performance during sudden demand changes.

Threshold-Based DVFS Model

Threshold-based DVFS improved upon static control by using processor utilization levels as decision criteria. Frequency increases when usage exceeds an upper threshold and decreases when usage falls below a lower threshold. This method was more responsive and easier to implement, making it popular in many early embedded systems. Nevertheless, fixed thresholds often failed under dynamic workloads. Rapid changes in utilization caused repeated switching between states, increasing instability and reducing efficiency. In addition, threshold values suitable for one application were often unsuitable for another.

Limitations Identified in Literature

A common observation across published studies is that conventional DVFS methods are increasingly inadequate for modern computing environments. Smartphones, wearable electronics, autonomous devices, and real-time embedded platforms generate workloads that change quickly and unpredictably. Software-controlled systems often respond too slowly, while fixed-threshold approaches cannot accurately represent workload diversity.

Another recurring concern is transition safety. In advanced VLSI circuits, frequency should not be increased before voltage reaches a safe level, and voltage should not be lowered before frequency is reduced. Many software-based DVFS systems cannot guarantee this sequencing with deterministic timing precision. Such unsafe transitions may introduce timing violations, instability, or reliability degradation.

Complexity is also a limiting factor. Although predictive and fine-grained methods offer theoretical advantages, their computational overhead, design cost, and integration challenges reduce practical adoption in constrained systems.

Shift Toward Hardware-Based Adaptive DVFS

Recent research strongly supports hardware-assisted power management solutions. Dedicated control logic can monitor workload activity and execute transitions far faster than software routines. FSM-based controllers are especially effective because they follow predefined transition states, ensuring reliable sequencing and repeatable timing behaviour.

Adaptive DVFS (ADVFS) extends this concept by continuously adjusting operating points based on real-time conditions rather than relying solely on static thresholds or periodic software sampling. Such architectures can deliver lower latency, improved stability, and higher overall energy efficiency. These characteristics make ADVFS suitable for next-generation processors, IoT systems, and battery-powered intelligent devices.

Block Diagram

The block diagram of the Adaptive Dynamic Voltage and Frequency Scaling (ADVFS) system illustrates the overall architecture used to optimize power consumption in processors, embedded systems, and System-on-Chip (SoC) devices. The proposed system uses a Finite State Machine (FSM)-based controller to monitor workload conditions and dynamically adjust voltage and frequency levels to achieve efficient system performance with reduced power usage. The architecture is composed of several interconnected functional modules that collectively implement intelligent runtime power management.

The operation begins with the Workload Input block, which represents the computational demand of the processor or digital system. This workload signal is commonly represented as load[2:0], where different binary values indicate low, medium, or high workload conditions. The workload information is continuously generated based on processor activity such as CPU utilization, instruction rate, or task queue occupancy. This signal serves as the primary input to the central controller.

The workload input is fed into the FSM-Based Adaptive DVFS Controller, which acts as the decision-making unit of the system. The controller continuously evaluates the workload condition and transitions between multiple operating states, generally labelled from S0 to S7. Each state corresponds to a predefined operating mode with a specific voltage and frequency combination. When the workload increases, the FSM moves to a higher performance state, resulting in increased voltage and clock frequency. When the workload decreases, the controller shifts to a lower power state, thereby reducing voltage and frequency to conserve energy. Based on the selected operating state, the FSM controller generates two important control outputs: voltage_level[2:0] and frequency_level[2:0]. These control signals determine the required power and performance settings for the processor.

The Voltage Controller receives the voltage_level[2:0] signal from the FSM controller. Its purpose is to convert the digital control value into an actual supply voltage suitable for system operation. The controller may interface with a voltage regulator or power management circuit to generate the required output voltage. It produces the signal voltage_out[3:0], which represents the selected voltage level supplied to the processor. This ensures reliable operation at the chosen performance state.

Similarly, the Frequency Controller receives the frequency_level[2:0] signal from the FSM controller and generates the required processor clock frequency. It may use clock divider circuits, multiplexers, or Phase Locked Loops (PLLs) to produce multiple clock levels. The final selected

clock is provided as the frequency_out signal, which determines the operating speed of the processor.

The Voltage Output and Frequency Output blocks apply the generated voltage and clock signals to the processor hardware. These outputs ensure that the system operates at the correct performance level while consuming only the necessary amount of power.

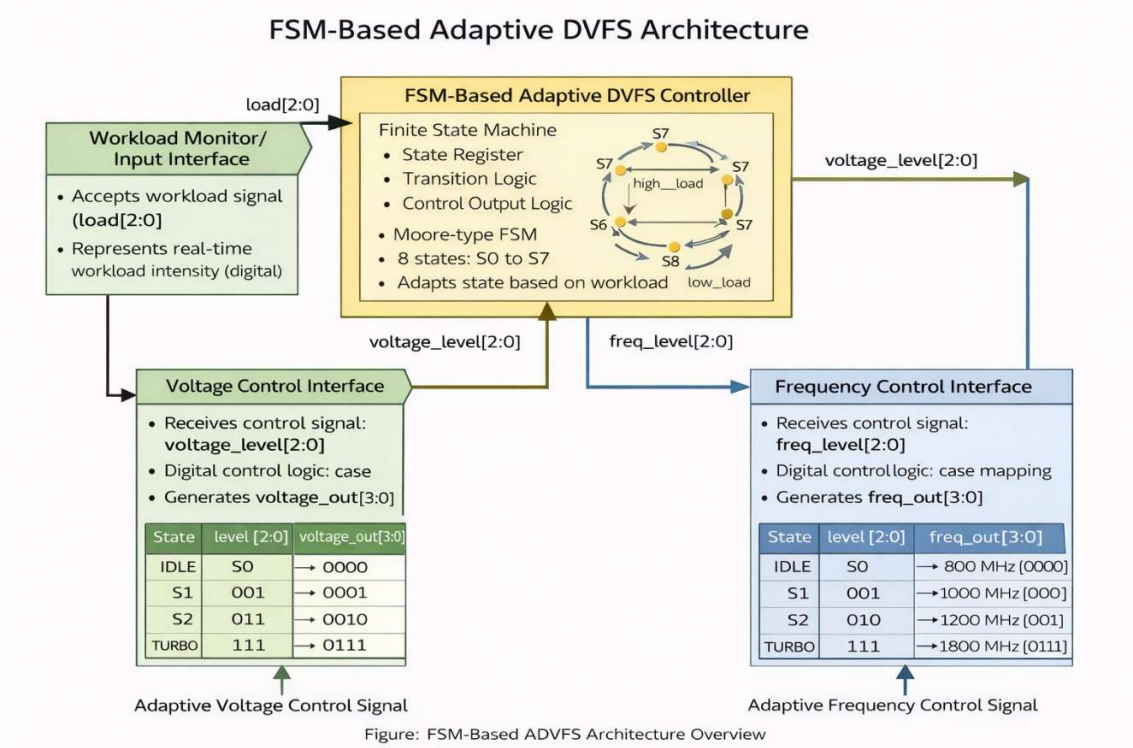

Figure 2; Block Diagram of Adaptive DVFS

IMPLEMENTATION

The implementation of the Adaptive Dynamic Voltage and Frequency Scaling (ADVFS) system is aimed at improving processor energy efficiency by dynamically modifying operating voltage and clock frequency according to workload demand. Instead of maintaining a constant performance level, the proposed system continuously adapts to changing computational requirements, thereby reducing unnecessary power consumption during light workloads while providing higher performance during intensive processing periods.

The ADVFS architecture is composed of several hardware modules that operate together in a coordinated manner. These modules include the Workload Monitoring Unit, FSM-Based DVFS Controller, Voltage Controller, Frequency Controller, Output Control Logic, and System Verification framework. Each module performs a dedicated function in the power management process. The workload monitoring unit detects processor activity, the FSM determines the appropriate operating mode, and the control modules adjust voltage and frequency accordingly.

The complete design is implemented using hardware description language techniques such as Verilog HDL, allowing accurate modelling, simulation, and synthesis for FPGA or ASIC platforms. Through coordinated operation of all modules, the ADVFS system achieves responsive and reliable runtime power management.

Workload Monitoring Module

The first stage of implementation is the workload monitoring module. This unit observes processor activity and estimates the current performance demand. It collects indicators such as CPU utilization, instruction execution rate, queue occupancy, or task request density. Based on these measurements, the module generates a digital workload signal that is used by the controller for decision making.

The workload condition is represented through a multi-bit encoded signal such as load[2:0], where different binary values indicate different utilization levels ranging from low to high workload states. This encoding simplifies communication between monitoring logic and the FSM controller.

For example, when processor activity is minimal, the module may generate 001, indicating a low-power operating condition. When heavy computational demand is detected, the module may generate 111, indicating that maximum performance may be required.

This module enables the system to react intelligently to workload variation and forms the primary input source for adaptive scaling decisions.

RESULTS AND ANALYSIS

The results obtained from the Adaptive Dynamic Voltage and Frequency Scaling (ADVFS) system clearly demonstrate the effectiveness of dynamically controlling processor voltage and frequency according to workload conditions. The primary objective of the proposed system is to minimize unnecessary power consumption during low workload periods while maintaining sufficient computational performance during high-demand conditions. By continuously adjusting the operating parameters in real time, the ADVFS system provides an efficient balance between energy savings and processing speed. In the implemented architecture, the workload monitoring module continuously observes processor activity and sends workload information to the FSM-based DVFS controller. Based on the received workload condition, the controller selects an appropriate operating state and generates corresponding voltage and frequency control signals. Simulation results confirm that the system successfully transitions between different operating modes according to changing workload requirements.

Output Waveform Analysis of ADVFS

The simulation waveform of the ADVFS system illustrates the dynamic behaviour of the controller during operation. The design was tested in the Vivado simulation environment, where important signals such as workload input, voltage output, and frequency output were monitored over time. At the beginning of the simulation, the workload input changes sequentially to represent different processor utilization levels. As the workload increases, the FSM controller detects the change and moves to higher performance states. Each state corresponds to a predefined voltage and frequency level. The waveform shows that the voltage output increases whenever the workload demand rises, indicating that the voltage controller successfully raises the processor supply voltage to support faster operation. Similarly, the frequency output also increases during high workload conditions, allowing the processor to run at a higher clock speed. Another important observation is that voltage and frequency changes occur in a synchronized manner. The system ensures that voltage is adjusted before frequency increases, thereby preventing timing violations and unstable operation. When workload demand decreases, both voltage and frequency outputs return to lower levels, demonstrating efficient power-saving capability.

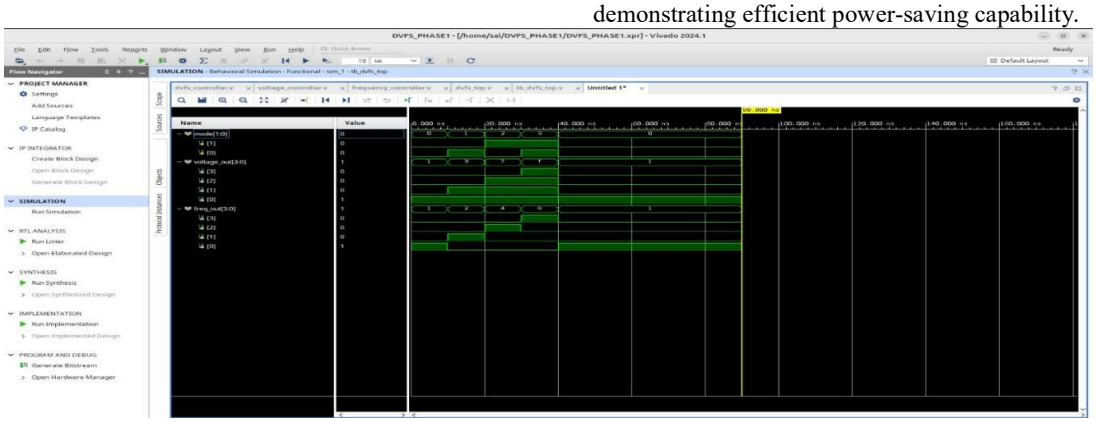

Figure 3; -Output Waveform of DVFS

Relation Between Workload, Voltage, and Frequency

The ADVFS system operates under multiple workload modes, where each mode corresponds to a specific voltage and frequency setting. During idle or low-power mode, the system uses the minimum voltage and lowest frequency to reduce power consumption. When light workload conditions are detected, the controller slightly increases both voltage and frequency to provide moderate performance. Under heavy workload conditions, higher voltage and frequency levels are selected to meet increased computational demand. During peak or turbo mode, the controller applies maximum voltage and frequency to achieve the highest possible performance. This operating behaviour confirms that the proposed ADVFS controller intelligently allocates processing resources based on workload intensity. As a result, the system avoids unnecessary energy consumption while maintaining performance when required.

Mode	Voltage Output	Frequency Output	Operating Condition
00	0001 (1)	0001 (1)	Idle / Low Power
01	0011 (3)	0010 (2)	Light Load
10	0111 (7)	0100 (4)	Heavy Load
11	1111 (F)	1000 (8)	Peak / Turbo

Figure 4; Relation between voltage, frequency vs corresponding operating conditions

FSM Output Analysis

The FSM output waveform confirms the correct functioning of the controller logic. Each state in the FSM represents a specific operating mode of the processor, and transitions occur according to workload changes. When the workload gradually increases, the FSM moves step-by-step from low-power states to higher performance states. Similarly, when workload demand decreases, the controller returns to lower-power states. The waveform shows that transitions occur in a stable and deterministic manner without illegal state changes or unpredictable behaviour. This validates that the FSM-based design is reliable for real-time power management applications. The use of FSM control also ensures safe voltage-frequency sequencing and fast response to workload variation.

Figure 5; Output waveform of FSM

RTL Schematic Analysis of ADVFS with Frequency Bank

The RTL schematic generated in Vivado confirms the structural implementation of the proposed ADVFS architecture. The design consists of several interconnected modules including the workload input logic, DVFS controller, frequency bank, voltage controller, and frequency selection circuitry. The workload mode signal is given as input to the central controller, which generates frequency select and voltage select outputs. The frequency bank receives the system clock and produces multiple divided clocks representing different performance levels. These divided clocks are then selected according to the controller output and supplied as the final processor clock signal. At the same time, the voltage controller produces the required supply voltage based on the selected operating mode. The RTL view confirms that the proposed architecture is modular, synthesizable, and suitable for FPGA or ASIC implementation.

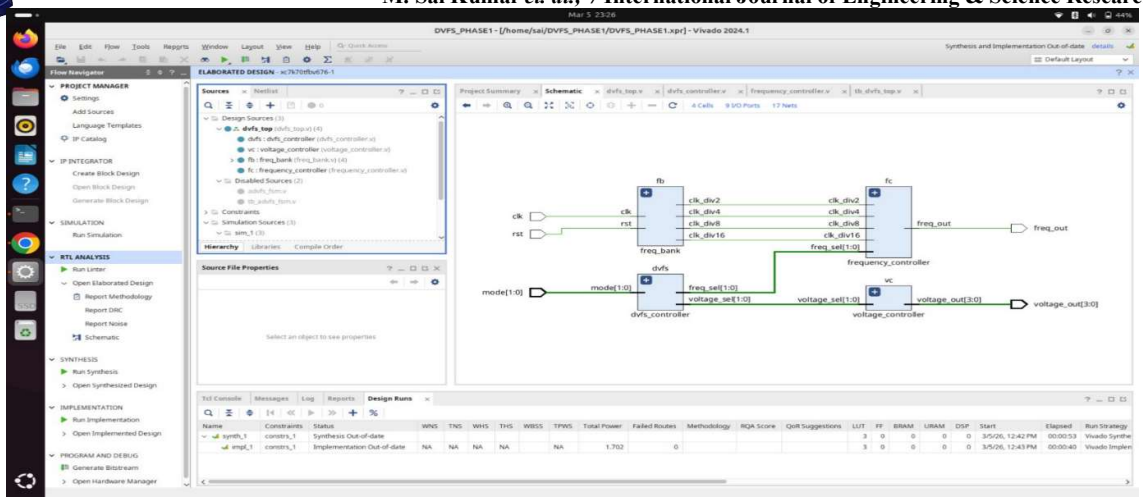

Figure 6; Schematic diagram of Adaptive DVFS with Frequency bank

Conclusion

Adaptive Dynamic Voltage and Frequency Scaling is an effective and intelligent power management technique for modern digital systems. By dynamically adjusting processor voltage and frequency according to workload demand, the proposed system minimizes unnecessary power consumption while maintaining required performance levels. In this work, an FSM-based ADVFS architecture was designed and implemented using modules such as workload monitoring, controller logic, voltage control, frequency control, and output sequencing blocks. Simulation results and RTL verification confirm that the system correctly transitions between multiple operating states according to workload variation. During low workload conditions, the controller selects lower voltage and frequency levels to conserve power. During high workload conditions, it activates higher performance modes to meet computational demand. This adaptive behaviour ensures an efficient balance between power savings and processing performance. Overall, the proposed ADVFS design provides a practical solution for processors, embedded systems, mobile devices, and industrial platforms where energy efficiency is essential.

Future Scope

Although the current implementation demonstrates successful adaptive voltage and frequency control, several improvements can be incorporated in future work. One important enhancement is the addition of temperature-aware control so that the system can respond not only to workload changes but also to thermal conditions. This would help prevent overheating and improve system reliability. Another useful enhancement is hysteresis-based control, which would prevent rapid switching between operating states when workload fluctuates near threshold values. Future versions may also support multiple governor modes such as performance mode, power-saving mode, and adaptive mode to optimize behaviour for different applications. Additional low-power techniques such as sleep states and clock gating can further reduce idle power consumption. Integration with PMIC acknowledgment signals would improve synchronization between voltage regulation and frequency transitions. An Operating Performance Point table can also be added to store optimized voltage-frequency combinations for different workloads. Finally, Unified Power Format based power intent modelling can be incorporated for advanced System-on-Chip implementation. With these enhancements, future ADVFS systems can become even more intelligent, efficient, and suitable for next-generation semiconductor technologies.

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