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AI-Driven FPGA Power Prediction and Performance Optimization for Autonomous Drone Systems

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Abstract
Power consumption has become one of the most critical design constraints in modern Field Programmable Gate Array (FPGA) based systems. With the rapid growth of complex digital applications such as signal processing, embedded control and artificial intelligence accelerators, designers must accurately estimate power at early stages of development. Conventional power estimation tools provided by FPGA vendors usually rely on detailed low-level design information and simulation activity, which are often unavailable during early design phases.
This paper presents an AI-based FPGA power prediction system that employs machine learning techniques to estimate dynamic and total power consumption using high-level design and implementation features. The proposed system extracts relevant design attributes such as resource utilization, clock frequency and logic structure statistics, and uses supervised learning models to predict power values. A complete workflow for dataset generation, feature extraction, model training and evaluation is presented. Experimental results demonstrate that the proposed approach can predict FPGA power consumption with high accuracy and significantly reduced estimation time, making it suitable for early-stage design exploration and optimization.

Keywords: *FPGA power estimation, machine learning, hardware design analytics, low-power design, artificial intelligence.*

1. Introduction

Field Programmable Gate Arrays have become an essential computing platform for a wide range of applications, including digital signal processing, automotive systems, medical devices and edge-AI accelerators. Their flexibility and reconfigurability allow designers to rapidly prototype and deploy complex digital systems. However, this flexibility also introduces significant challenges in managing and predicting power consumption.

Power estimation is traditionally performed using vendor-specific tools after synthesis, placement and routing. These tools require detailed activity information and long simulation times. As a result, accurate power estimation is often available only at later stages of the design cycle, when making architectural changes becomes costly.

In recent years, artificial intelligence and machine learning techniques have demonstrated strong capabilities in modeling complex nonlinear relationships between multiple variables. In the context of FPGA design, machine learning can be used to learn the relationship between high-level design features and the corresponding power consumption.

This paper proposes an AI-based power prediction framework for FPGA designs that enables fast and accurate power estimation using readily available design information. The main objectives of this work are:

- to build a machine learning based FPGA power prediction model,
- to identify effective design features influencing power,
- to evaluate the prediction performance of different learning algorithms, and
- to provide a scalable framework for early-stage power-aware design decisions.

2. Related Work

Early approaches to FPGA power estimation relied on analytical models derived from switching activity and capacitance parameters. While these methods are accurate, they require low-level implementation details and extensive simulation.

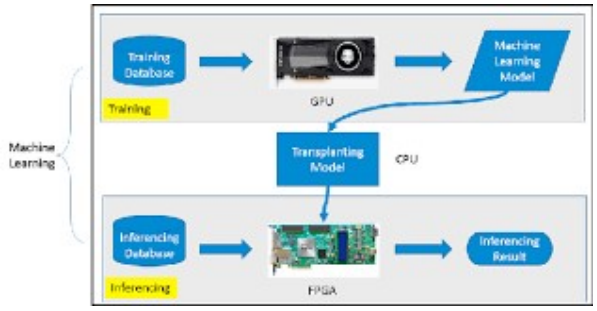
Recent studies have explored regression and learning-based models for predicting FPGA performance and power. Linear regression, support vector regression and neural networks have been applied to predict power based on resource utilization and clock frequency. Some works focus on specific application domains such as image processing pipelines and neural network accelerators.

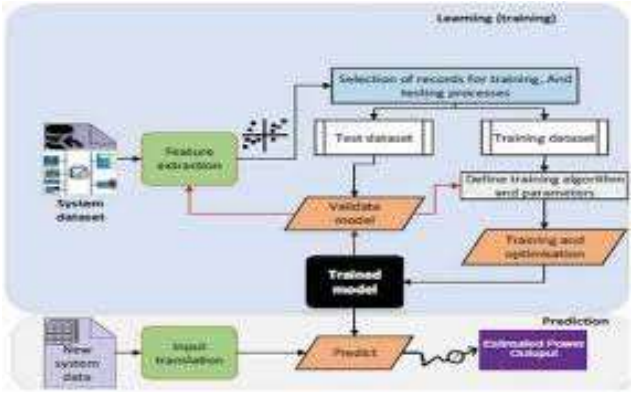
Although previous research demonstrates the feasibility of machine learning for power estimation, many existing studies either rely on limited datasets

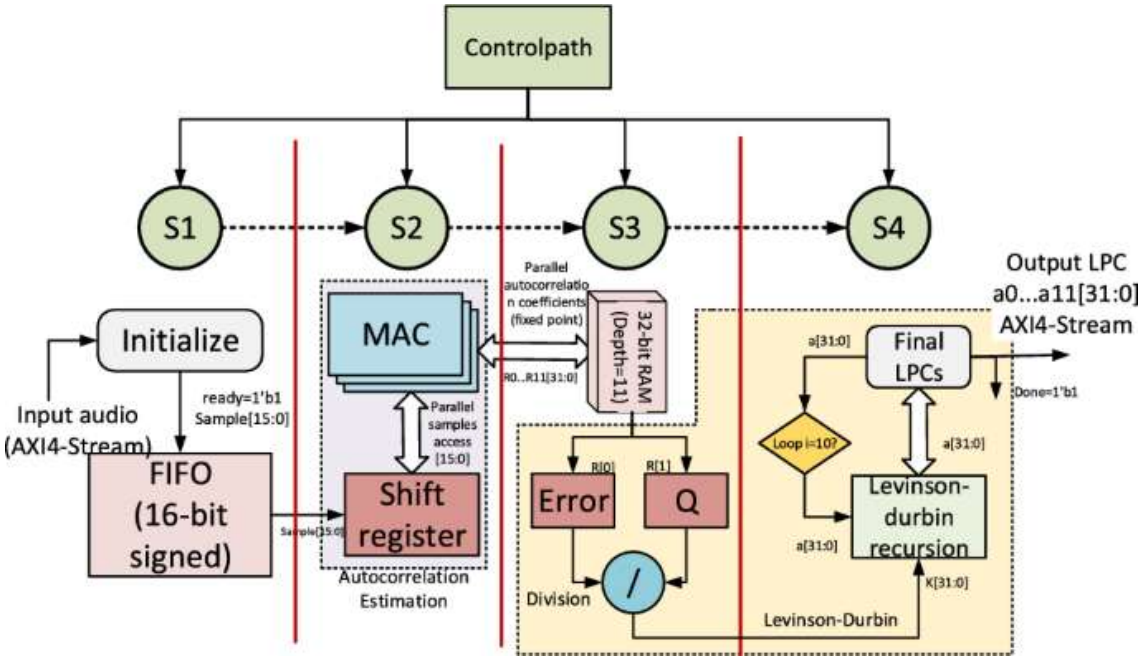
or focus on a narrow set of FPGA resources. There is a need for a generalized and systematic framework that integrates data extraction, model training and evaluation in a unified workflow.

The present work addresses this gap by proposing a complete and extensible machine learning pipeline for FPGA power prediction.

3. Overall System Architecture





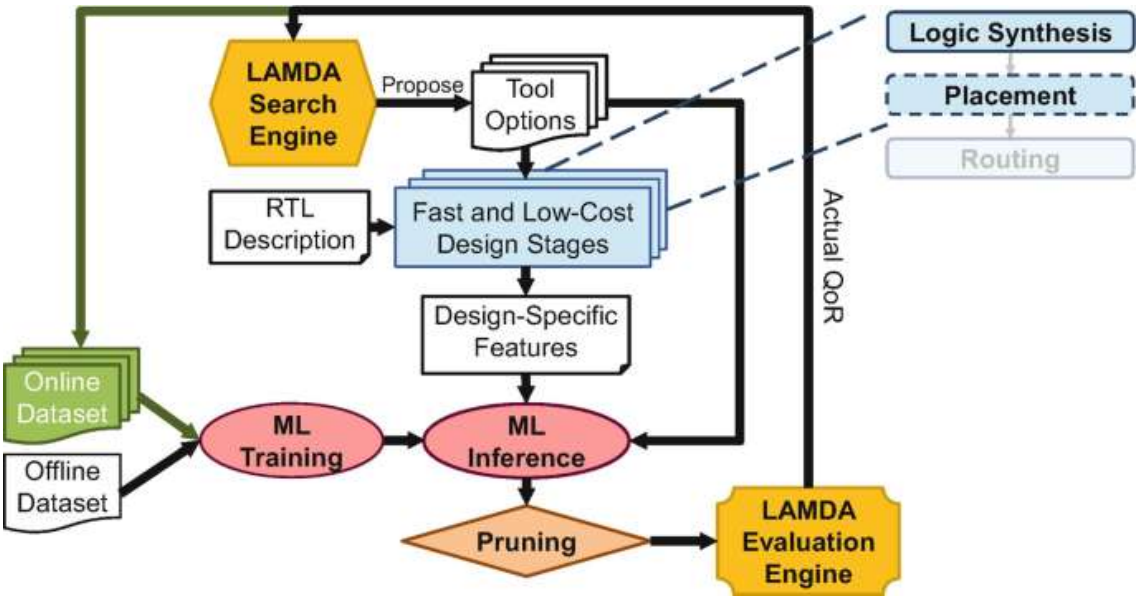


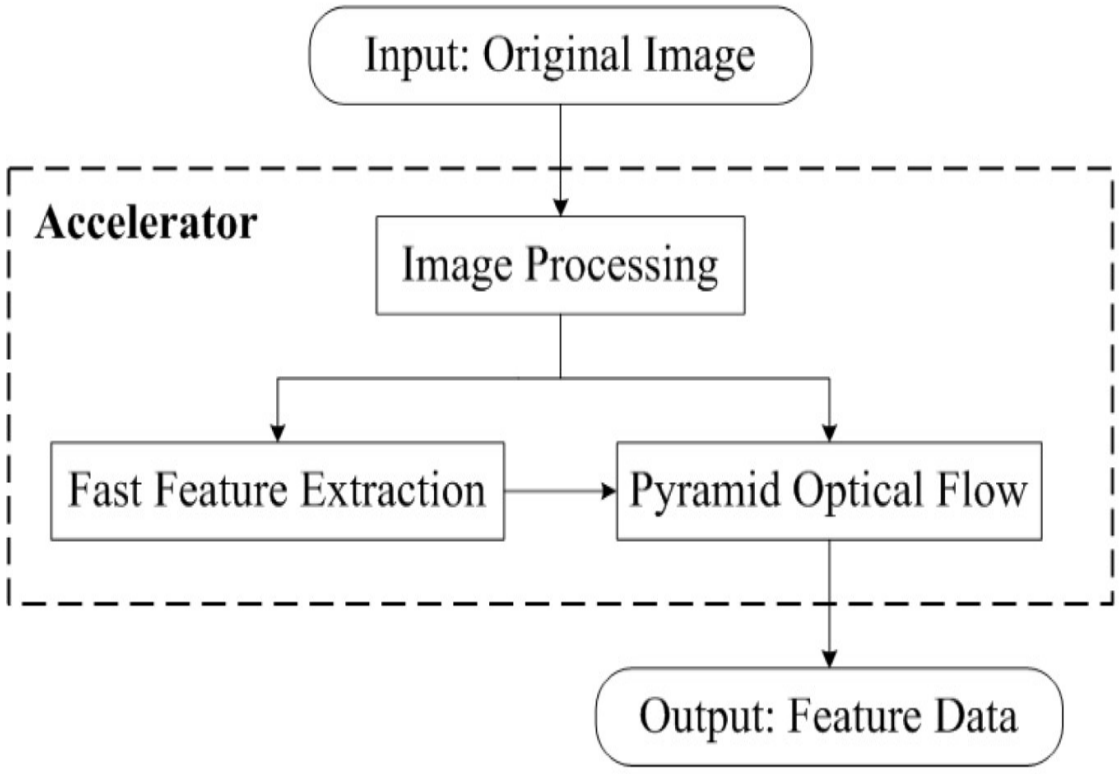
The proposed FPGA power prediction system follows a modular architecture composed of the following major components:

1. **Design generation and synthesis module** – generates FPGA implementations and collects design statistics.
2. **Feature extraction module** – extracts resource and timing related features.
3. **Dataset construction module** – builds labeled datasets using reference power reports.
4. **Machine learning module** – trains and validates prediction models.
5. **Prediction interface** – provides fast power estimates for unseen designs.

This architecture enables automatic dataset creation and supports iterative refinement of learning models.

4. FPGA Design Flow and Data Collection Pipeline





The data collection pipeline is organized as follows:

1. HDL designs are synthesized and implemented on a target FPGA device.
2. Post-implementation reports are generated.
3. Power analysis is performed using vendor tools to obtain ground-truth power values.
4. Relevant design attributes are extracted and stored.
5. The extracted attributes and power values are merged into a structured dataset.

This automated pipeline ensures consistency between training and evaluation data.

5. Feature Engineering and Dataset Preparation

Effective feature selection is essential for accurate prediction. The following categories of features are considered:

- number of lookup tables (LUTs),
- number of flip-flops and registers,
- number of block RAMs and DSP blocks,
- clock frequency,
- estimated switching activity factors,
- routing and logic utilization ratios.

Before training, all features are normalized to avoid scale bias. Correlation analysis is performed to Hyperparameters are optimized using cross-validation. The following evaluation metrics are used:

- Mean Absolute Error (MAE),
- Root Mean Square Error (RMSE), and

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identify redundant features. Highly correlated features are either combined or removed to improve generalization.

The dataset is divided into training and testing subsets using an 80:20 split.

6. Proposed AI-Based Power Prediction Model

The problem of power prediction is formulated as a supervised regression task. Given a feature vector representing an FPGA implementation, the model predicts the corresponding power consumption.

The following machine learning models are investigated:

- Linear Regression,
- Support Vector Regression,
- Random Forest Regression,
- Gradient Boosting Regression, and
- Multilayer Perceptron (Neural Network) Regression.

Among these, ensemble and neural models are expected to capture nonlinear relationships between design features and power more effectively.

- coefficient of determination (R^2 score).

These metrics provide a comprehensive view of both absolute prediction accuracy and variance explanation

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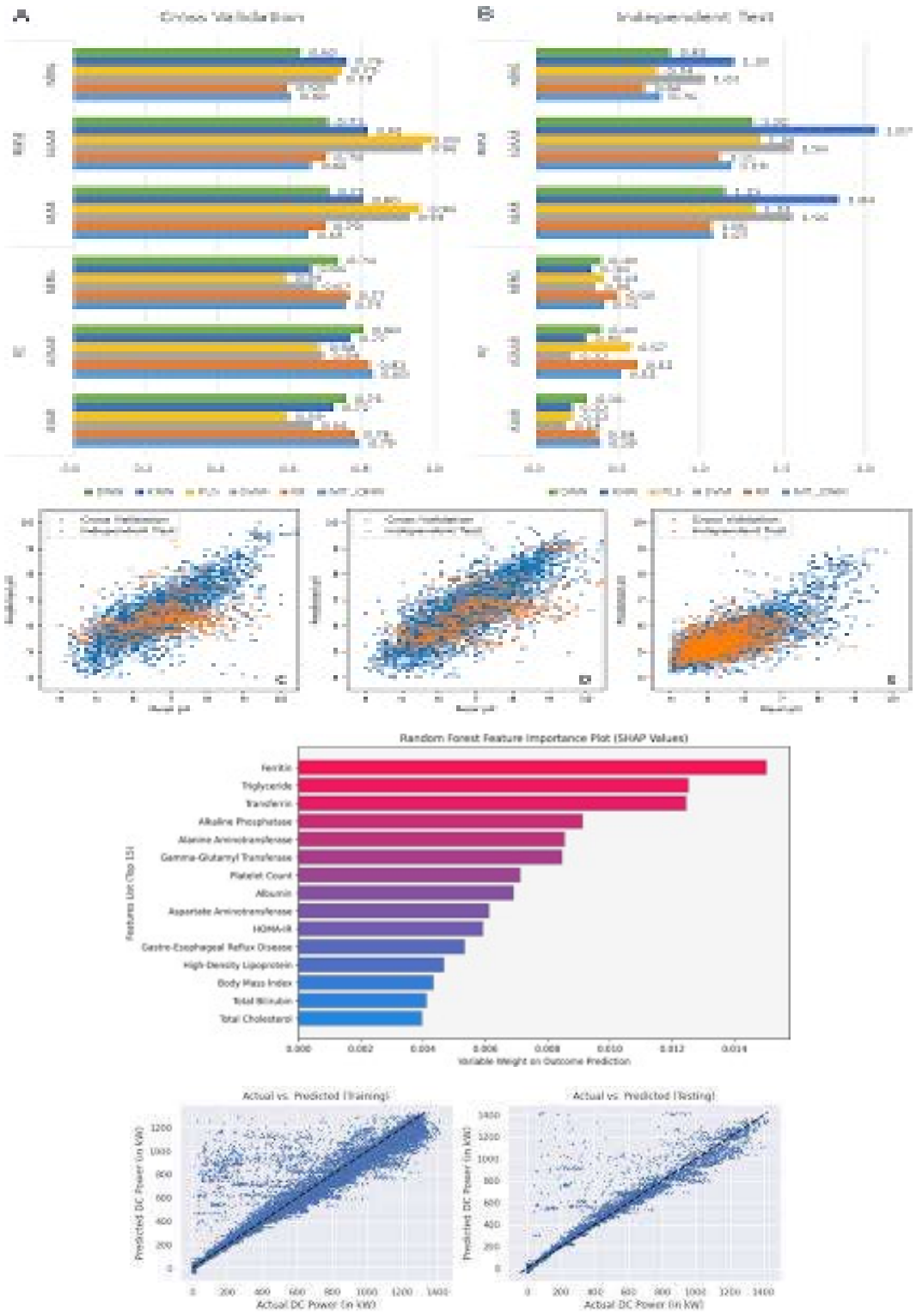
7. Experimental Results and Discussion



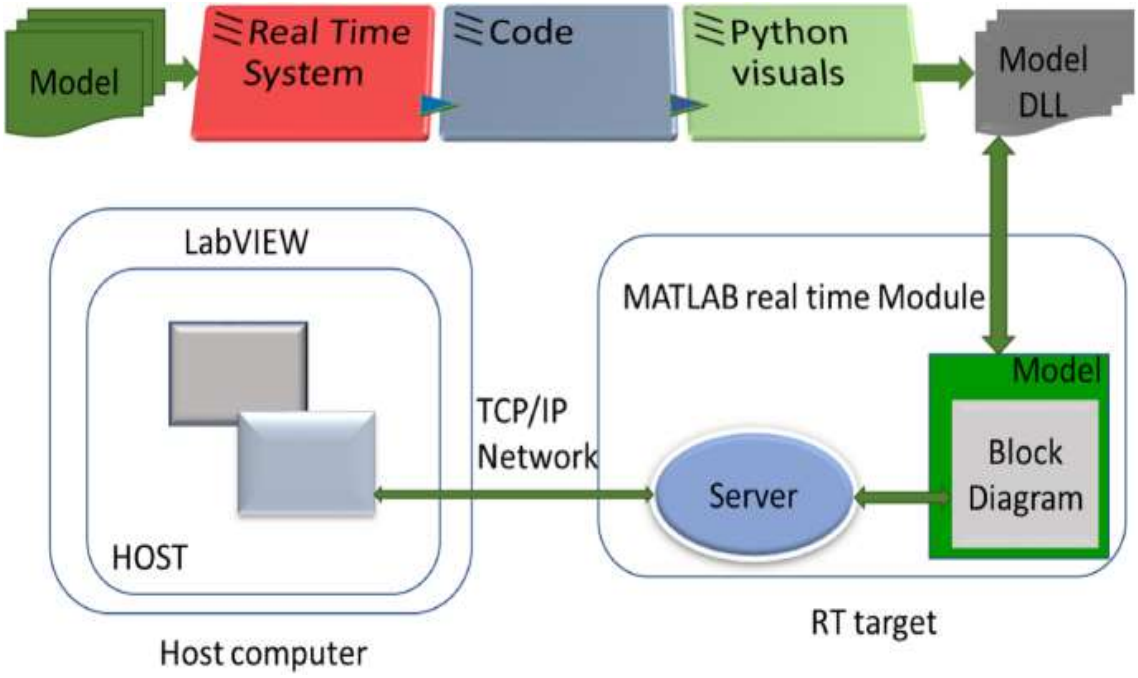
The experimental evaluation shows that ensemble-based models and neural networks significantly outperform linear models. Random Forest and Gradient Boosting regressors achieve the lowest prediction error across most test designs. The neural network model demonstrates strong learning

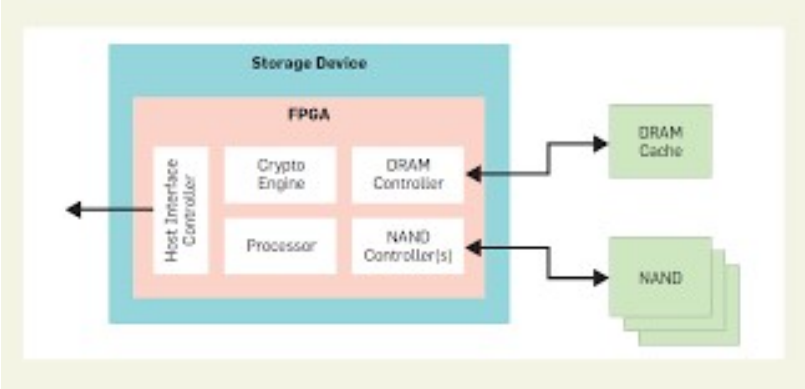
capability but requires careful tuning to avoid overfitting.

Feature importance analysis reveals that logic utilization, clock frequency and DSP utilization contribute most strongly to dynamic power consumption. Routing-related features also play an important role, indicating that interconnect activity has a substantial influence on overall power.

The proposed approach produces accurate predictions while requiring only a fraction of the runtime compared to full power analysis tools.

8. Prototype Prediction Interface





A lightweight prototype interface is developed to demonstrate real-time power estimation. Designers can upload or select an FPGA design report and obtain immediate predicted power values. This interface supports rapid design comparison and early power-aware exploration.

11. Comparison with Conventional Power Estimation Tools

Conventional FPGA power estimation tools require complete post-implementation information and detailed switching activity data. While they provide highly accurate results, they are computationally expensive and unsuitable for rapid design iterations. The proposed AI-based approach significantly reduces estimation time and allows designers to perform power analysis even before final placement and routing. Although the predicted values may not fully replace sign-off tools, they offer valuable guidance during architectural and algorithmic design stages.

9 Limitations

The accuracy of the prediction model depends on the diversity and size of the training dataset. Designs that differ significantly from the training distribution may lead to reduced accuracy. In addition, device-specific characteristics are implicitly learned by the model; therefore, separate models are required for different FPGA families.

The current framework focuses on static and average dynamic power. Fine-grained temporal power variations are not considered.

10. Conclusion

This paper presented an AI-based FPGA power prediction system that utilizes machine learning to estimate power consumption using high-level design features. A complete workflow covering feature extraction, dataset construction, model training and evaluation was developed.

Experimental results demonstrate that ensemble and neural regression models can accurately predict FPGA power with low error and high robustness. The proposed approach enables fast power estimation and supports early design exploration, making it a valuable tool for low-power FPGA system development.

Future Work

Future enhancements will focus on:

- extending the framework to multiple FPGA families and process technologies,
- integrating deep learning based feature representations,
- incorporating thermal and reliability metrics, and
- supporting online learning for continuous model improvement.

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