VALIDATION AND IMPLEMENTATION OF N-BIT DIGITAL CMOS BASED LOW POWER HIGH SPEED COMPARATOR

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Abstract - *The most fundamental arithmetic comparisons in a digital comparator involve comparing two numbers that are greater than, less than, or equal to each other. While doing enormous level arithmetic comparisons, a digital comparator needs more space, which results in higher power consumption and a delayed response. This can be solved by using N-bit comparator with two modules using 45 GPDK CMOS Technology. An N-bit comparator can operate at extremely high speeds having effective area and power dissipation which can also reduce the proposed comparator design's space and power consumption. The proposed model is carried out bitwise starting with the least significant bit and working way up to the most significant bit. This process continues only if the bits are equivalent, and the result is what is known as a Parallel prefix tree structure. Two distinct modules make up the proposed comparator structure methodology which are Final unit (FU) and comparison evaluation unit (CEU) are the first and second units, respectively. Validated findings from the methodical organization of repeating logic cells are used to create tree structures. The FU module authenticates the result by relying on CEU results. The proposed architecture's use of structured VLSI technique enables area derivation using analytical method relating transistor count and total delay, which can be understood in terms of operand bit width. While running the virtuoso simulations at 1 GHz with both old model and 45 GPDK CMOS technology, it has been found that the design has been enhanced the operating speed by 31.92% while reducing power usage by 77.76%.*

Keywords: - *Domino, Pass Transistor, Transmission Gate Comparator, Power dissipation, Area, Delay, Parallel prefix tree structure, 45 GPDK CMOS Technology.*

1. INTRODUCTION

CMOS N-bit digital Using comparators is essential for this project. Two binary numbers used, and compared based on their magnitude. There is a possibility that one of the two numbers will be bigger, less, or equal to the other. A digital circuit known as a digital comparator performs the operation of comparing two binary numbers. The digital comparator is the backbone of many different types of designs. output is derived from a process that includes comparison. This output is used to determine the final findings.

Some of them include Applications Digital picture processing, pattern recognition and matching, arithmetic classification, data compression, and neural networks. networks are all examples of artificial intelligence.

networks. more with built-in testing features, signature analyzers, and jitters measurement). Digital comparator is a fundamental building block in each of the aforementioned applications. The major element employed is an optimized comparator design for improving general-purpose memory addressing logic in computer architecture. widespread implementations of computation-based architectures. As a result, there is a requirement for maximum efficiency in terms of velocity, size, and strength. Some comparator designs employ dynamic logic to adhere to the standard of lower power usage. However, due to limitations, limited speed, and low noise margin, dynamic designs become difficult to implement. Some of the other ideas are accomplished utilizing flat adder circuits with subtractors in combination with specialized logic circuits.

Two distinct modules make up this proposed comparator structure methodology. Final unit (FU) and comparison evaluation unit (CEU) are the first and second units, respectively. Validated findings from the methodical organization of repeating Using logic cells, one may make hierarchical diagrams. The FU module authenticates the result by relying on CEU results. The proposed architecture's use of structured VLSI technique area may be derived from the number of transistors used and the total delay incurred, both of which are expressed in terms of the bit width of the operand. Spectre simulations have been carried out at 1 GHz using 0.18-micron CMOS technology. When compared to the old model, the proposed design enhanced operating speed by 31.92% while reducing power usage by 77.76%.

2. LITERATURE REVIEW

This chapter discusses the project's literature review. The area may be analytically derived as a function of the overall delay experienced in input-output flow and the overall number of transistors thanks to the consistent extremely extensive integration topology highlighted in the proposed architecture.

This paper introduces an N-bit register that has low power consumption, high throughput, and small physical footprint. digital comparator. There are two distinct modules in the suggested comparator structure One can begin with the CEM (comparison evaluation module) and end with the FM (final module). second. CEM stages consist of the recursive logic cells used to construct a prefix tree in simultaneously., independent of the input operand bit widths. On the basis of the CEM's findings, the FM certifies the final comparison.

The area may be analytically derived as a function of the overall delay experienced in input-output flow and thanks to the consistent extremely extensive the suggested architecture's integration topology is emphasized, and a total number of transistors are listed. has been reduced. Results from specter simulations at 1 GHz using CMOS technology with a 0.18 m lateral dimension have been presented. When compared to existing comparators created utilizing CMOS The proposed comparator uses 180 nm CMOS and 64-bit against 0.18 m complementary metal-oxide semiconductor technology. exhibits low power dissipation (1.03 mw), low input-output latency (0.57 ns), and low fan-out-of-4 delay (9.5 ns). Pipelining and power-down techniques are cited as comparable for achieving higher throughput and lower power usage. It has been suggested that the high fan-in throughput of the pipeline can be attributed to N-transistor dynamic technology is used in the comparator design. operation.

operation. CMOS logic. Some have put forth the idea to utilize a different structure with using a magnitude-decision logic based on a priority encoder to speed up operations.

To reduce a lengthy dynamic logic chain and reduce delay This architecture makes use of two pipelined operations, one on each clock edge. Jitter margin and clock frequency, however, are further constrained by the heavily loaded clock signal, rendering the structure not conducive to broad evaluation. Large operand comparator bit widths, which consists of two comparator stages, is reported in. The output of the second stage's decoder is delivered to a priority encoder and an 8-to-1 multiplexer. first stage's 8-bit comparisons, which are then transmitted there to help choose the right first-stage outcome. In order to perform two-stage actions in a single clock cycle and make it easier operations must be timed to the clock's rising and lowering edges. the comparator uses two-phase domino clocking.

Presenting the Hamming weights of two vector inputs, or a binary vector and a constant, can be compared with certain new counting-based algorithms. It is demonstrated that the suggested comparators outperform the finest completely digital systems in terms of speed and simplicity for intermediate vector lengths. These gains in A faster and cheaper population count is achieved by combining comparison and counting processes with parallel accumulative and up/down counters, which also improves accuracy. View. Vector of binary digits V = v1, v2,..., vn's HAMMING weight, which is defined as H(V)=1invi, is a value ranging from 0 to n. A binary vector Another binary vector of any length, U = u1, u2,..., um, is needed for some applications that compare H(V), or the number of 1s in the vector V, to a threshold value k or H(U). Choosing between H(V) k and H(V) H(U) exists is, thus, fundamental to the questions at hand. These advantages are the result of two enhancements: Counting people using multiple counters simultaneously method that is more effective and the phase of population counting being combined with the phase of comparison.

3. CONVENTIONAL METHODOLOGY

The fundamental logic gate creates first. The transmission gate creates all logic gates. The 4-bit comparator circuit connects the necessary logic gates in order to build the 4-bit comparator.

A. Transmission Gate Design

First, A transmission gate using NMOS and PMOS transistors created, connected in parallel. The transmission gate is fundamentally an AND gate. A resistor is attached to the output terminal of the Transmission gate since its output is unreliable. At the complementary NMOS and PMOS gate terminals, control signal A is applied. If the Logic 1 is input, and the command signal is logic.

Input logic 1 turns on PMOS and turns off NMOS, while logic 0 turns off PMOS and turns on CMOS. If The output will be logic 0 if the control signal is logic 0. inverse of what was input. In the following circuit schematic, the NMOS transistor is ON and the PMOS transistor The NMOS transistor is disabled and the output current can flow through it when the control signal is a logic 1. The output current is conducted by the PMOS transistors

when the control signal is logic 0, turning off the NMOS. Logic 0 at the input turns off PMOS and turns on CMOS. activated. The logic of the control signal state of '0' indicates that the output is equal to the control, and vice versa.

B. And Gate Design

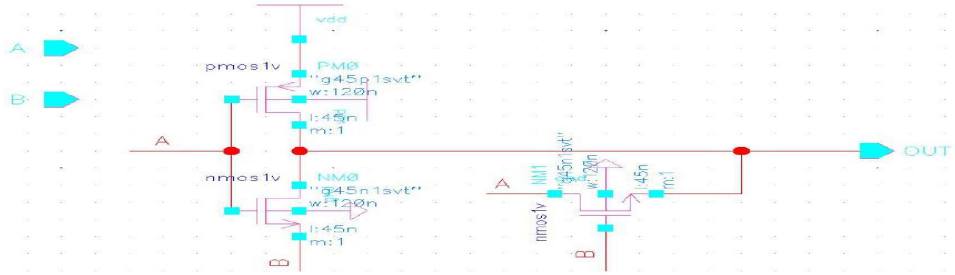

Figure 1: XOR gate using TG

Figure 4.2 displays the transmission gate's circuit diagram, which includes 4 PMOS, 4 NMOS, 1 resistor, 1 inverter, and 1 control input. It functions because the NAND gate needs fewer components than the CMOS gate. thus, by using a two input thus gate, create a three input AND gate. 4 input AND gates and 5 input AND gates can be designed similarly.

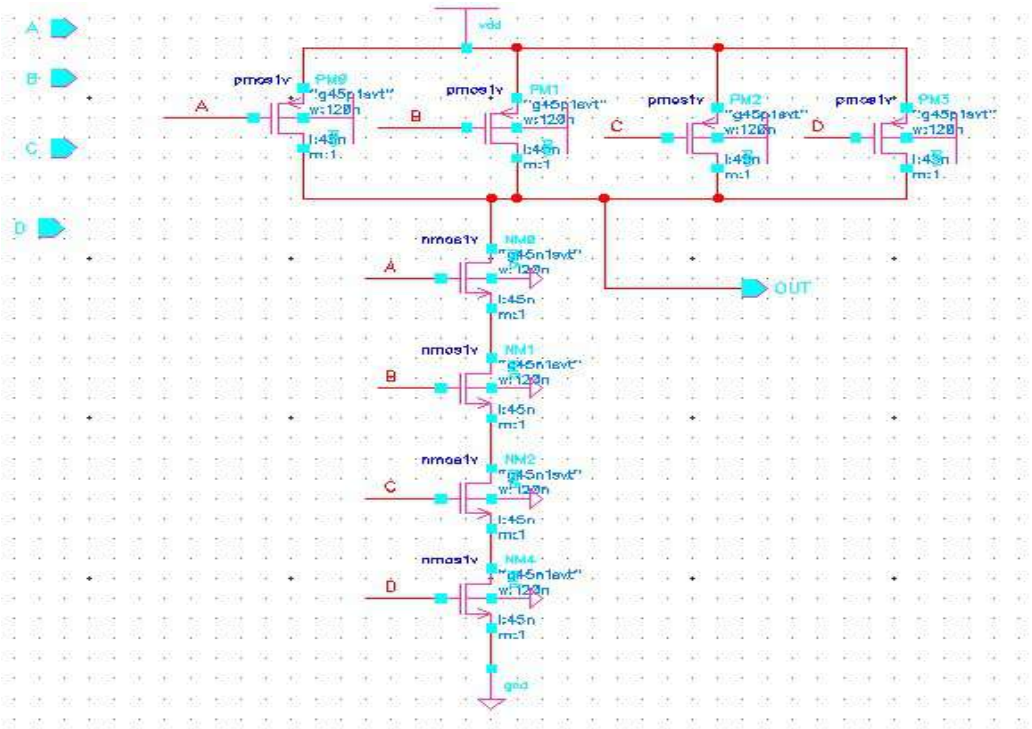

Figure 2: 4 input AND gate

4. PROPOSED METHOD

4.1 Introduction

The proposed strategy and presented a schematic of it in this section.

Block Diagram

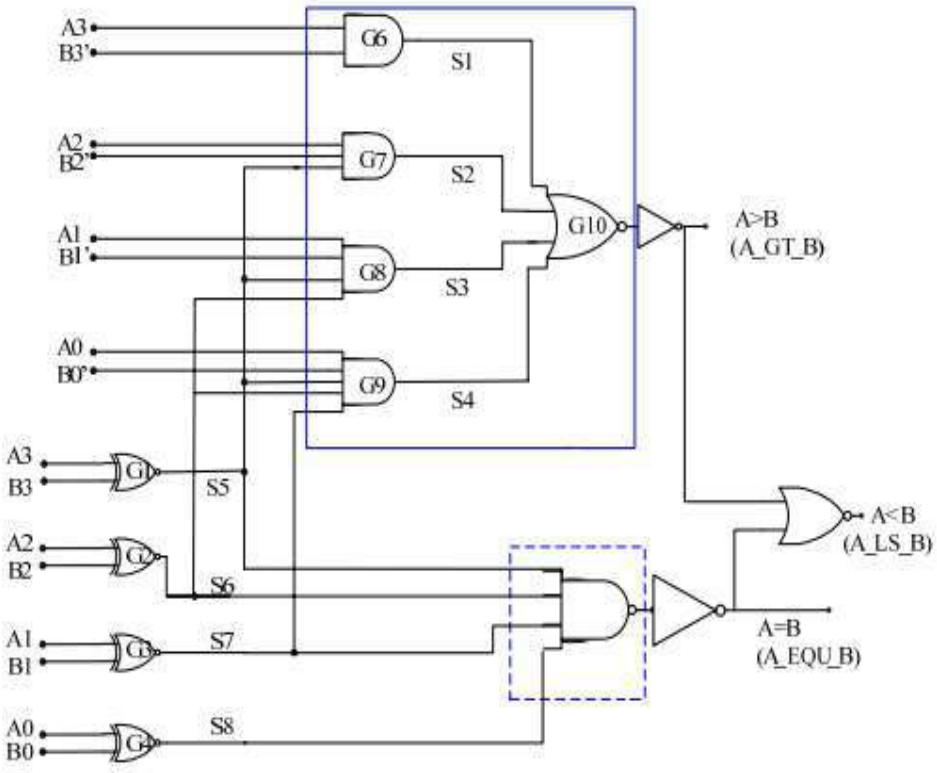

Figure 4.1: Diagram of the proposed scheme

In order to lower the space no of gates can be reduced. The above circuit can be made simpler by the logic of AB and A=B, as shown in figure. As you can see from the diagram above, in addition to the inverters, the 4-Bit comparator using 11 gates can also br created. Gates of this type include XOR, AND, and NOR. The four XOR gates are identical. Although the number of inputs for the five AND gates vary, the basic concept remains the same. The NOR gate also does.

The circuit shown above uses a variety of AND gates.

The circuit consists consisting of four XOR gates, five AND gates accepting inputs ranging from two to five, four inputs, and two outputs. NOR inputs and 5 inverters, as can be seen from the simplified logic diagram. Time and space were chosen by the measures of performance to be used in the design process. Taking into account the use of performance metrics such as td, tphl, tplh, area, power dissipation, and others metrics demonstrates that

area is advantageous for pseudo-Nmos. Propagation delay, Tr, and Tf are all aspects of temporal performance that can take into consideration in this project. propagation was chosen as the first index because, This the SS1 block is far more complex than the remainder of the circuit, as seen by the simplified logic diagram. components. The size start with is Wp_eff=1.73Wn_eff. To make Tr equal to Tf in previous blocks, Wp_eff= 3Wn_eff was used. From the design (figure 2.5) it was observed that the circuit utilizes a 4 input NOR. Generally, it is known how expensive NOR gates are.

4.2 XNOR circuit and simulation

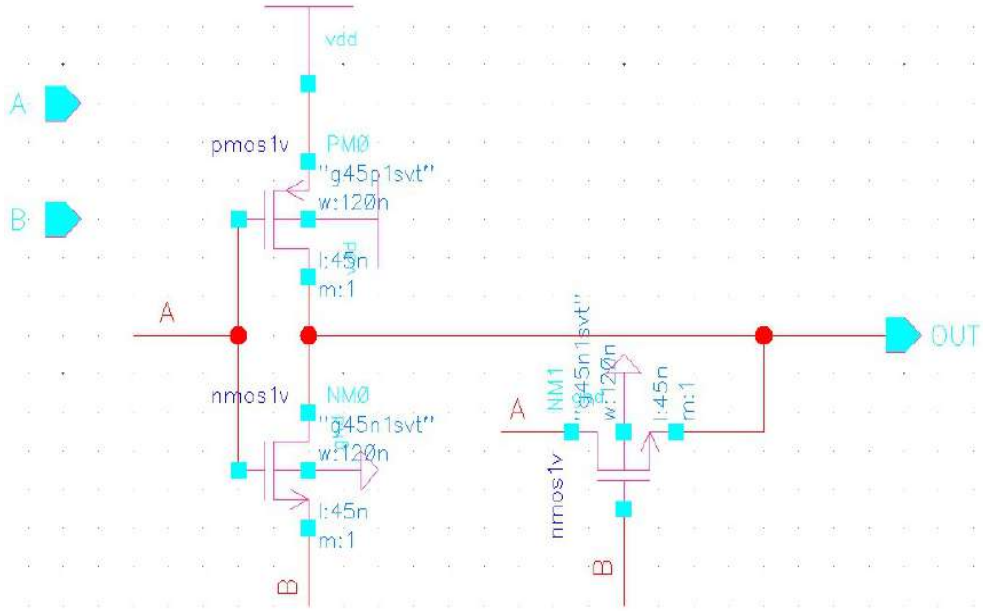

Figure 4.2: Diagram of the proposed scheme

This places more strain on the driver circuit in terms of space, Power, delay, output load capacitance (as a result of input capacitance and drain diffusion capacitance both increase as drain temperature rises. are all affected... for the same performance. Normally, switch to NAND and avoid using a big fan in NOR. However, since the fan-in for this project is only 2, 2 inputs NOR gates are used for practice, and test the performance to obtain precise information with which to compare the characteristics. Here, the XNOR, NOR, SS1, and SS2 components of the comparator design were shown and measure it after simulation.

A. XOR GATE DESIGN USING PASS TRAN

First, XOR gate was created using NMOS and PMOS transistors connected in parallel. The transmission gate functions essentially as an AND gate. A resistor is attached to the output terminal of the Transmission gate since its output is unreliable. At the complementary NMOS and PMOS gate terminals, control signal A is applied. When the When the input and control signal are both logic zero, CMOS is turned on and PMOS is turned off, but when the input and control signal are both logic one, PMOS is turned on and NMOS is turned off. If the Whenever the control signal is a logic zero, the result is inverted. what was input.

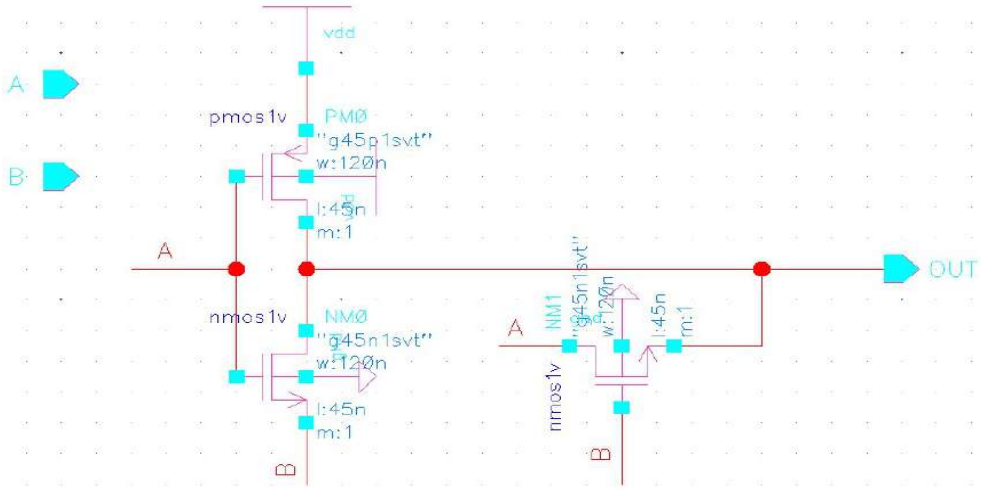

Figure 4.3: XOR gate using PASS TRANSISTORS

In the following circuit schematic, both the NMOS and PMOS transistors are active. OFF when the control signal is logic '1', allowing output current to travel in an NMOS transistor's direction. The output current is carried by the PMOS when the control signal is logic 0, when the NMOS is disabled. transistors. Furthermore, PMOS is disabled and CMOS is active. when the input is logic "0." Logic '0' on the control signal means that the output is equal to the control, and vice versa.

B. AND GATE DESIGN USING TRANSMISSION GATE

Figure 5.4 displays the transmission gate's circuit diagram, which includes 4 PMOS, 4 NMOS, 1 resistor, 1 inverter, and 1 control input. It functions because the NAND gate needs fewer components than the CMOS gate. Thus by using a two input gate, can create a three input AND gate. 4 input AND gates and 5 input AND gates can be designed similarly.

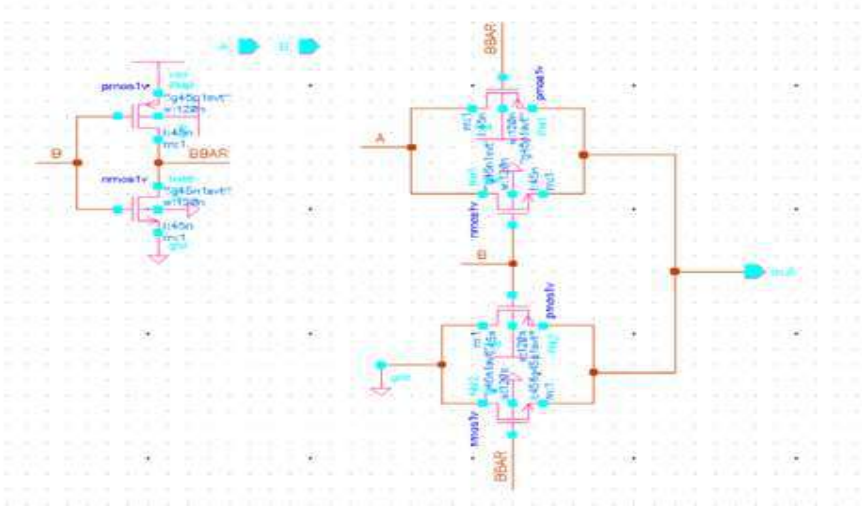

Figure 4.4.1 2 input AND gate

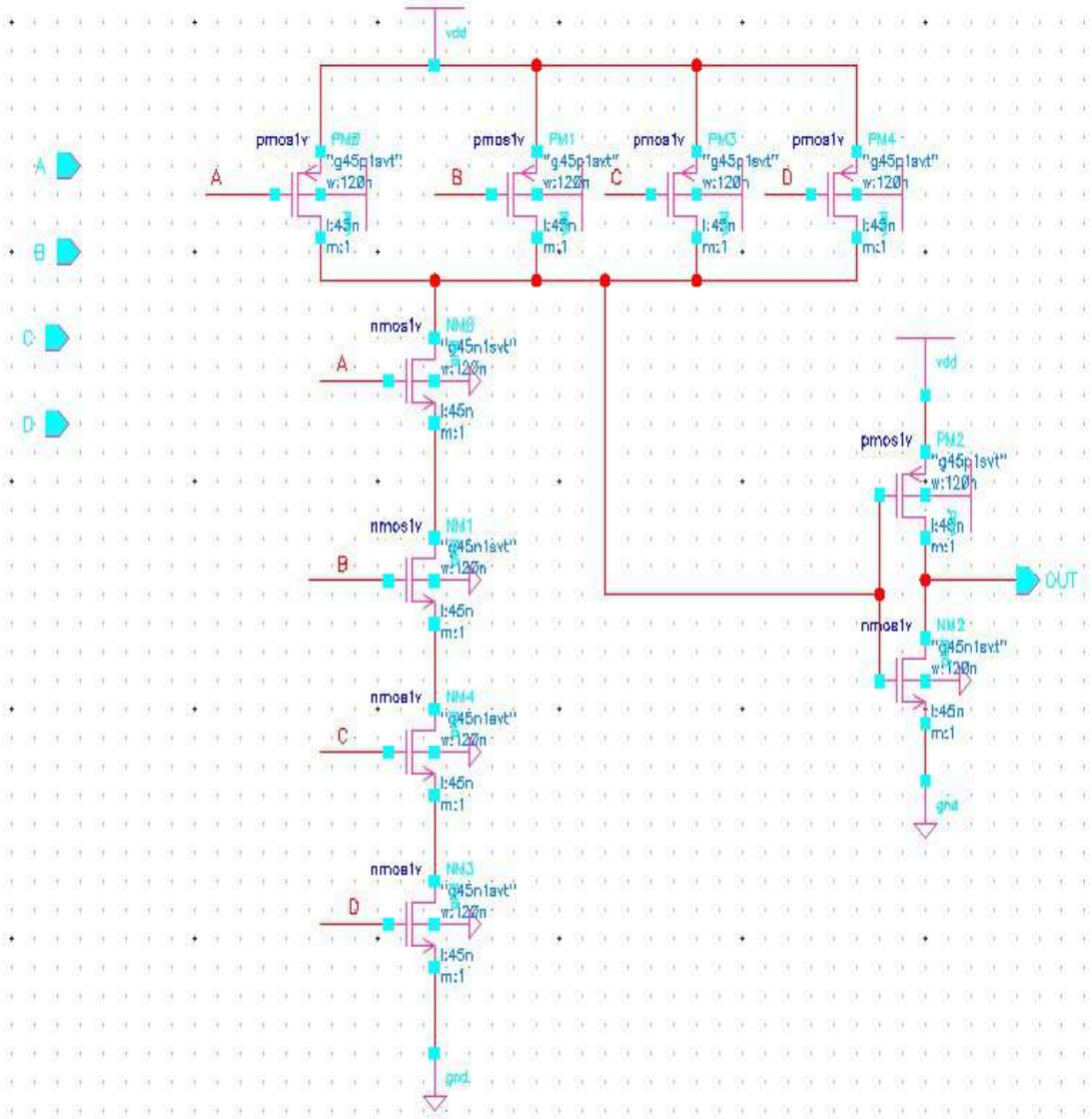

Figure 4.4: 4 input AND gate

5. RESULTS

5.1 Introduction

This chapter discussed about the simulation results of 4-bit comparator.

5.2 Experimental Results

5.2.1 Schematic level design and simulation

The circuit consists of Four XOR gates, five AND gates that take inputs from two to five, four inputs, and two outputs. NOR inputs and five inverters, as can be seen from the simplified logic diagram. Select both time and location as optimization metrics. during design. Despite the fact that pseudo-NMOS has an advantage in terms of area, it is not used until respective parameters like td, tphl, tplh, area, power dissipation, were suitable and

others were taken into account variables are analyses the factors. Propagation delay, Tr, and Tf are all aspects of temporal performance that take into consideration. The propagation was chosen as first index because, as the SS1 block, this simplified logic diagram reveals that the complexity of this circuit is far higher than the other components. The size that starts with is Wp_eff=1.73Wn_eff. To make Tr equal to Tf Initially, Wp_eff= 3Wn_eff was applied to other blocks, from the designed (figure 2.5) it was illustrated that the circuit utilizes a 4 input NOR.

5.3 XNOR circuit and simulation

These circuits have two problems despite using only three transistors and not requiring complimentary inputs. Take the 3T-XNOR gate from Fig. 6.1 as an example. The complete circuit functions as a standard inverter when transistor M3 is off and input B is at a high level, allowing the complement form of input A to pass to the output. However, the issue arises when input B switches to logic '0'. The output level matches the absolute threshold value (|VTP|) of a pMOS transistor when A = B = 0.

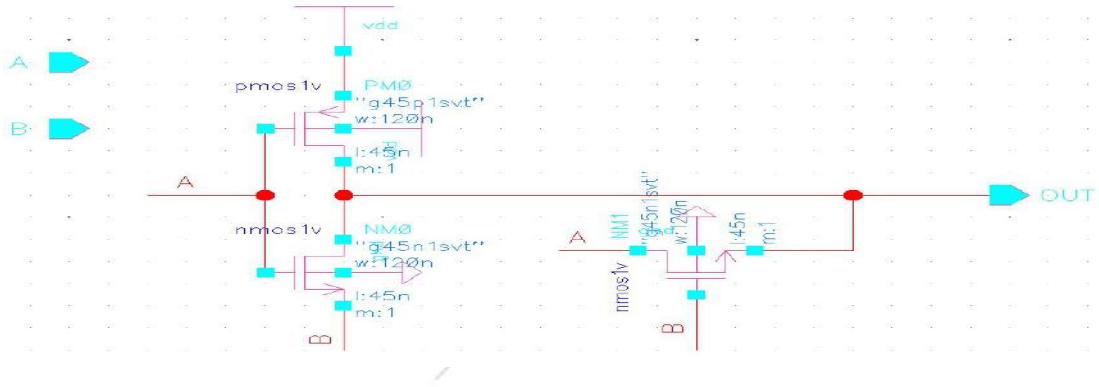

Figure 5.1: XNOR schematic

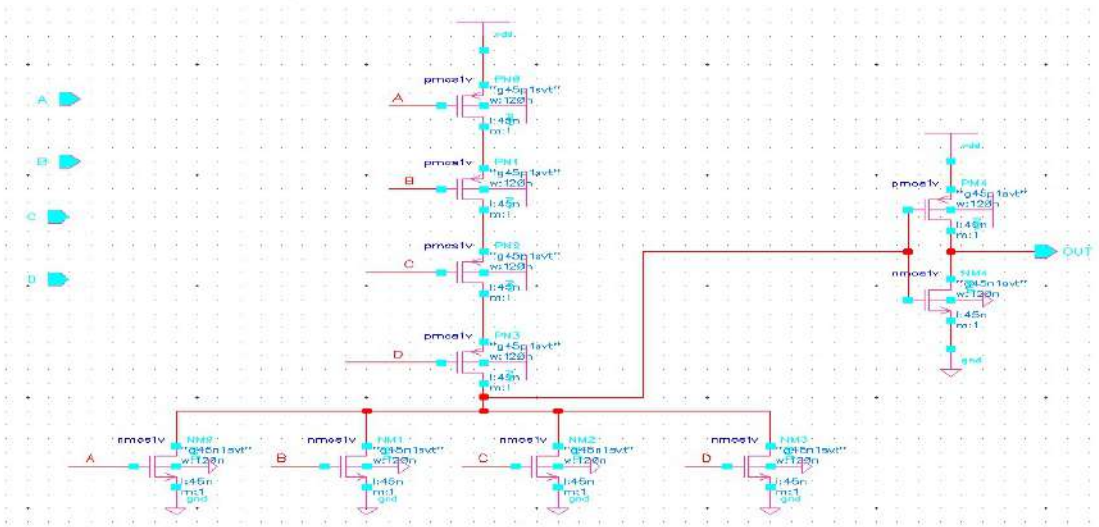

Figure 5.2: 4 inputs OR schematic diagram

5.4 INPUT OR circuit and simulation

Before creating In order to design an inverter with equal rise and fall time, two-input NAND, NOR, XOR, and XNOR gates must be used. The mobility gap between electrons and holes must be adjusted for. In silicon, electron mobility is approximately 2.5-3 times greater than hole mobility. Because of this, the pMOS transistor's must be set to W/L ratio i.e 2.5 times higher than the nMOS transistor's in order to have equivalent rise and fall periods in an inverter. After completing this assignment, we must size each gate's transistors under the worst possible charge/discharge resistances Rc/Rd input combination constraints.

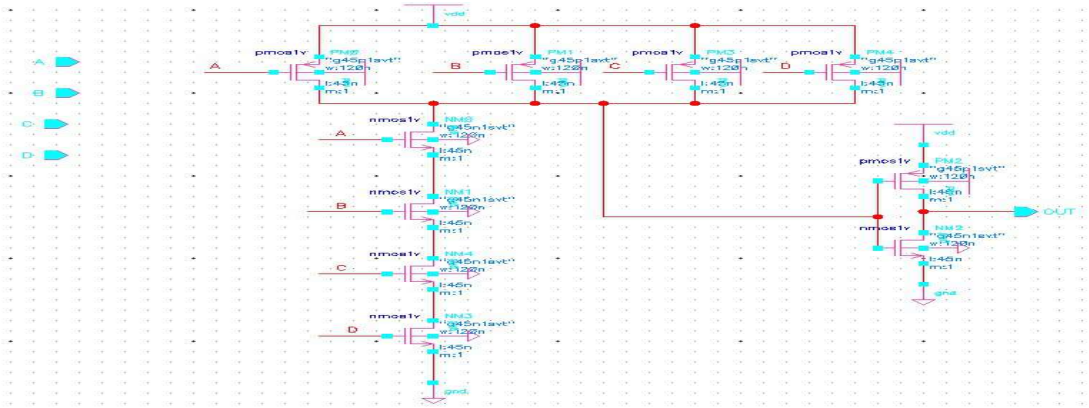

Figure 5.3: 4 inputs AND schematic diagram

5.5 4 input AND Gate schematic

The PUN and PDN each supply the maximum ON resistance for the rise and fall times of each gate circuit, respectively.) The maximum charging state of a NAND gate is scenario is when only one pMOS is turned on, while discharging only occurs when both nMOS are turned on. Rc/Rd = 1/2 in the worst-case scenario. Consequently, in an effort to strike a middle ground between the two streams (and account for their varying degrees of movement).

5.6 5 Input AND gate schematic

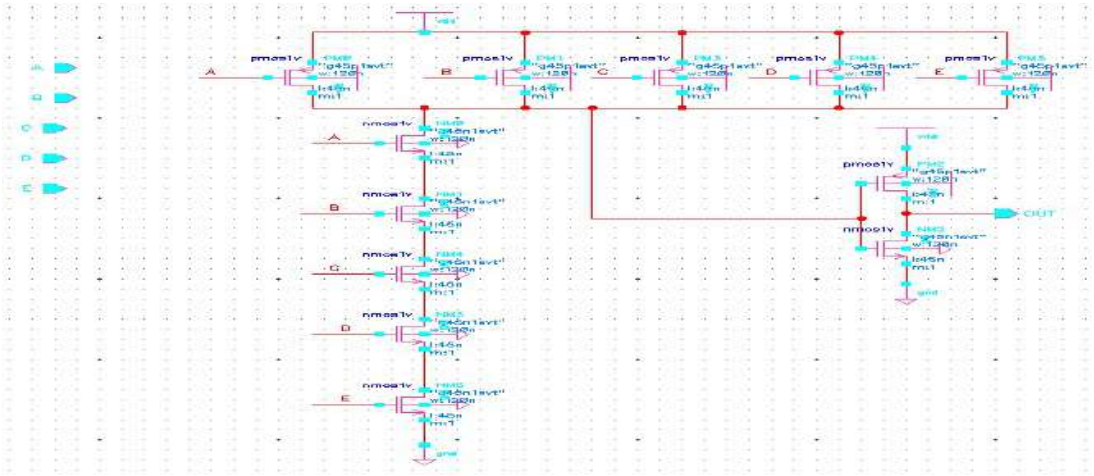

Figure 5.4:5 inputs AND schematic diagram

Conclusion

A scalable comparator is opted in this study employing comparative evaluation and modules. Parallel prefix tree structure is accomplished by using reiterated logic cells, which are a regular structure in the CEM. Using regular structure for any arbitrary bit widths, the characteristic predictions of proposed comparator is evaluated. It was found that incorporating 45 GPDK CMOS resulted in the working frequency being highest with the least amount of delay and the lowest amount of power dissipation. Because of these benefits, the opted comparator is preferred for a variety of applications, including scientific calculations and memory addressing logic.

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