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Cascode Cross-Coupled Stage High Speed Dynamic Comparator

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ABSTRACT

This Project proposed a CMOS Three modelled comparator and its new version to enhance the speed and reduce the noise. When validate with conventional comparators this proposed comparator will enhance additional amplification structure, with this the efficiency of the proposed model will increase enormously, In proposed model an extra signal has been configured in the regeneration stage, in turn will enhance the speed of the proposed circuit will increase further. To validate the proposed model, using 45nm BSIM4 Model. By comparison, proposed model dictates that three stage circuits enhance speed by 34% and dwindles noise by several times. The proposed model has been validated through Mentor graphics 45nm BSIM4 Technology.

1-INTRODUCTION

Analog-to-digital converters (ADCs) are widely used in various applications due to the increased demand for mixed-signal systems. The comparator, an essential block in ADCs, plays a vital role in determining the speed and accuracy of the ADCs. The performance of an ADC relies on the robustness of the comparator, especially for low noise, low-power, and high-speed operations. Dynamic comparators are preferred in low-power and high-speed designs due to their zero static power. They are classified as single tail (ST) and double-tail (DT) topologies. Various ST circuits are reported to suffer from tradeoffs between energy consumption (EC), offset, and speed. ST topology also suffers from large kickback (KB) noise and requires a large voltage headroom since the input transistors are directly stacked with the latch stage. Due to these drawbacks, the DT configuration is preferred for the design of high-speed comparators. Designing a high-speed comparator that can resolve small input difference voltages while holding on to the high-speed capability over a wide range of common-mode voltage is challenging. The conventional DT comparator reported has mitigated the drawbacks of the ST comparator. However, it fails to give valid outputs for small input difference voltages. This has a direct impact on the resolution of ADCs. Moreover, at higher common-mode levels, the performance of the conventional DT comparator degrades because the input pair enters the triode region without providing sufficient gain. A dynamic comparator resistant to common-mode variations with the delayed operation of the latch is presented in. However, it requires a large area and suffers from increased KB noise. Furthermore, the insufficient preamplifier gain makes it impractical to use in high-precision ADCs. In the dynamic bias DT comparator presented in the preamplifier partially discharges the drains of the input transistor pair to reduce EC. However, the speed is compromised to attain energy efficiency. To improve the latch regeneration time, a transconductance-enhanced latch stage is presented. It has the same drawback as the conventional DT comparator in its common mode performance. Additionally, due to stacking in the latch stage, the delay increases swiftly for lower supply voltages. Our work targets to reduce the comparator delay by enhancing the preamplifier gain compared to other high-speed DT architectures

reported. The performance improvement is achieved by including a cascode cross-coupled pair in the preamplifier stage. The circuit is designed and implemented in a 65 nm CMOS technology with a 1.1 V supply. The proposed technique offers better delay performance throughout the input voltage range, especially at smaller input differences. Also, the cascode cross-coupled pair alleviate the delay degradation at higher common-mode voltages. These advantages make the proposed comparator suitable for high-speed, high-resolution ADCs.

The conventional DT dynamic comparator has an input stage and a latch stage that have separate tail transistors. Two independent tail currents enable us to optimize the tradeoff between speed, offset, and EC. This topology has fewer transistors stacked, making it suitable for low-voltage applications. It also reduces the KB noise due to the isolation between the input transistors and the output nodes. In the conventional DT, at smaller input difference voltages (1VIN), the latch is unable to sense the differential voltage due to the limited differential gain of the preamplifier. The proposed comparator mitigates this drawback by lowering the common-mode voltage and improving the differential voltage at the preamplifier output.

we presented a novel DT comparator topology suitable for high-speed applications. It consists of a cascode cross-coupled pair, which increases the preamplifier gain in the comparison phase. Furthermore, the common-mode voltage at the preamplifier output is lowered by the cascode cross-couple pair. As a result, the latch regenerates quickly. Post layout simulations in a 65 nm CMOS technology with a supply of 1.1 V confirmed that the delay is reduced considerably without much increase in the EC compared to the state-of-the-art architectures.

2-LITERATURE SURVEY

The literature on high-speed dynamic comparators reveals various techniques aimed at optimizing performance, particularly in high-speed applications such as analog-to-digital conversion and signal processing. Early designs of comparators primarily focused on static comparators, which provide stable outputs but suffer from higher power consumption and slower switching speeds. To overcome these limitations, dynamic comparators, which use pre-charge and decision phases, were developed to minimize power usage while improving speed.

Key advancements in dynamic comparator design include the incorporation of cross-coupling in the comparator stage. Cross-coupling improves the speed by introducing a feedback mechanism between transistors, effectively accelerating the decision-making process. The dynamic nature of these comparators allows them to operate with low power consumption by only consuming power during the decision phase, unlike static designs that continuously consume power. Several studies have focused on the trade-offs involved in dynamic comparators, such as the limited output swing, which can restrict the range of signals the comparator can handle. Research also addresses the need for reducing offset voltage in these comparators, as small mismatches in transistor characteristics can lead to inaccuracies. Techniques like input calibration and dynamic offset correction have been explored to mitigate these errors. Furthermore, modern research investigates optimizing noise immunity and improving the comparator's robustness under various operating conditions. The integration of compensation techniques and the careful design of the feedback mechanism are critical to achieving stable and reliable performance in high-speed environments. Overall, the cross-coupled stage high-speed

dynamic comparator represents the latest evolution in comparator technology, combining low power consumption, high speed, and reliability, and is suitable for applications that demand minimal delay, such as in high-speed ADCs and communication systems.

3-SOFTWARE IMPLEMENTATION

Technologies Used (EDM)

Tanner EDA is a suite of tools for the design of integrated circuits. These tools allow you to enter schematics, perform SPICE simulations, do physical design (i.e., chip layout), and perform design rule checks (DRC) and layout versus schematic (LVS) checks. There are 3 tools that are used for this process: S-edit – a schematic capture tool T-SPICE – the SPICE simulation engine integrated with S-edit L-edit – the physical design tool Using S-Edit (Schematic Entry Tool) & T-SPICE (Analog Simulation Tool).

Curves of an NMOS Transistor S-edit are a schematic entry tool that is used to document circuits that can be driven forward into a layout of an integrated circuit. It also provides the ability to perform SPICE simulations of the circuits using a simulation engine called T-SPICE. T-SPICE can be setup and invoked from within S-edit.

Initially Setup your Directory Structure & download Libraries a) Log onto a computer on 6th floor Cob Leigh. B) You want to create a directory for all of your Tanner EDA projects. You also will need to download and unzip a set of library & model files from the course website that will be used for your simulations. – Create a directory structure named "EELE414_VLSI_Fall2011\Tanner Projects c) Go to the course website and download the zip file called "Tanner_Libraries.zip". Unzip it into your Tanner Projects directory. These groups of files contain the necessary information to enter components into S-edit (circuit symbols), perform SPICE simulations (models), and do physical layout (layer definitions, DRC, LVS).

Start S-Edit:

Start – All Programs – Tanner EDA – Tanner Tools v12.6 – S-Edit v12.6.

Start a New Design:

Using the pull-down menus, create a new design: - File – New – New Design A dialog will appear asking for a design name and location. When you give the name, S-edit will create a folder of that name in the directory that you provide that will contain all of the design files. You should give a descriptive name that represents each simulation you will be running. – Enter the name "HW03_NMOS_IV_Part1" and browse to your "EELE414_VLSI_Fall2011\Tanner Projects" directory – Click "OK".

Create a new Cell:

A "cell" is a design element. A cell can contain multiple views such as schematics and symbols. Cells can be instantiated in other cells. When performing a simulation, we will typically call the cell "TOP". When we are testing a circuit, for example an inverter, the inverter will have its own cell that contains a schematic of the devices and a symbol. The inverter cell is instantiated in the TOP cell that contains ideal elements such as voltage sources and probes that are only used for simulation. This allows us to separate the cells that are actually going to be implemented on the die versus cells that are only used for simulation. Using the pull-down menus, create a new cell view: - Cell – New View: - enter the cell name "TOP". Ensure the design name is "HW03_NMOS_IV_Part1" and click OK. You can leave the interface and view names "view0". A blank schematic page will appear. It is a good idea to save this right now.

PHASE 1: CASCODE CROSS-COUPLED STAGE HIGH SPEED DYNAMIC COMPARATOR USING 15T

In this chapter we will discuss about Existing and proposed systems of Cascode Cross-Coupled Stage High Speed Dynamic Comparator using 15T.

Existing System

Analog-to-digital converters (ADCs) are widely used in various applications due to the increased demand for mixed-signal systems. The comparator, an essential block in ADCs, plays a vital role in determining the speed and accuracy of the ADCs. The performance of an ADC relies on the robustness of the comparator, especially for low noise, low-power, and high-speed operations. Dynamic comparators are preferred in low-power and high-speed designs due to their zero static power. They are classified as single tail (ST) and double-tail (DT) topologies. Various ST circuits are reported to suffer from tradeoffs between energy consumption (EC), offset, and speed. ST topology also suffers from large kickback (KB) noise and requires a large voltage headroom since the input transistors are directly stacked with the latch stage. Due to these drawbacks, the DT configuration is preferred for the design of high-speed comparators. Designing a high-speed comparator that can resolve small input difference voltages while holding on to the high-speed capability over a wide range of common-mode voltage is challenging. The conventional DT comparator reported has mitigated the drawbacks of the ST comparator. However, it fails to give valid outputs for small input difference voltages. This has a direct impact on the resolution of ADCs. Moreover, at higher common-mode levels, the performance of the conventional DT comparator degrades because the input pair enters the triode region without providing sufficient gain. However, it requires a large area and suffers from increased KB noise. Furthermore, the insufficient preamplifier gain makes it impractical to use in high-precision ADCs. In the dynamic. bias DT comparator presented in the preamplifier partially discharges the drains of the input Manuscript received 24 June 2022; revised 1 December 2022, 1 February 2023, and 25 March 2023; accepted 23 April 2023. Date of publication 23 May 2023; date of current version 28 June 2023. (Corresponding author: Komala Krishna.) The authors are with the School of Electrical Sciences, Indian Institute of Technology Goa, Ponda 403401, India (e-mail: krishna183422003@iitgoa.ac.in; npnandakumar@iitgoa.ac.in). Color versions of one or more figures in this article are available at https://doi.org/10.1109/TVLSI.2023.3276000.

Digital Object Identifier 10.1109/TVLSI.2023.3276000 transistor pair to reduce EC. However, the speed is compromised to attain energy efficiency. To improve the latch regeneration time, a transconductance-enhanced latch stage is presented. It has the same drawback as the conventional DT comparator in its common mode performance. Additionally, due to stacking in the latch stage, the delay increases swiftly for lower supply voltages. Our work targets to reduce the comparator delay by enhancing the preamplifier gain compared to other high-speed DT architectures reported. The performance improvement is achieved by including a cascode cross-coupled pair in the preamplifier stage. The circuit is designed and implemented in a 65 nm CMOS technology with a 1.1 V supply. The above Schematic of the Existing double tail comparator with cascode cross-coupled pair to enhance preamplifier gain. The cascode cross-coupled pair made up of M3, M4, Mc1, and Mc2 improves the preamplifier performance.

A PMOS cross-coupled pair is employed to increase the differential gain of the preamplifier. To enhance

the performance further, the proposed topology, shown in figure 3.1, introduces a cascode cross-coupled pair made up of M3, M4, Mc1, and Mc2. As a result, a higher difference voltage, 1V f n, f p, at the preamplifier output nodes (f n, f p) is observed by the latch. This helps to reduce latch regeneration time and to resolve for smaller 1VIN. Operation: During the reset phase (CLK = 0), the tail transistors MT 1 and MT 2 are off along with the cascode transistors Mc1 and Mc2. The switching transistors Ms1 and Ms4 charge the f n and f p nodes to VDD. Similarly, Ms2 and Ms3 charge the drain nodes of M3 and M4 to VDD. Therefore, M3 and M4 are off. The transistors MR1 and MR2 ensure a proper start condition for the comparator.

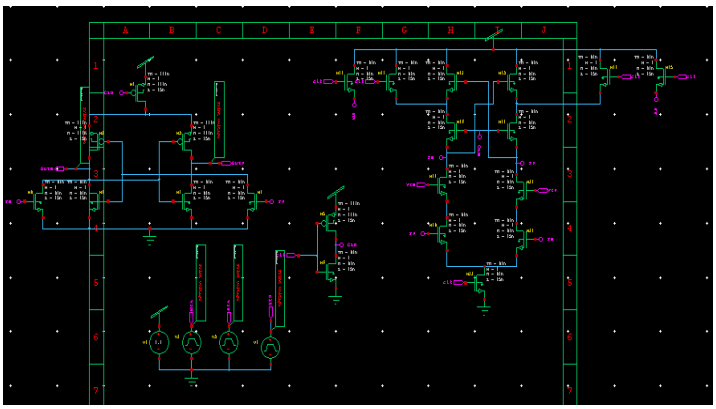

Fig3.2: Schematic of existing method

During the comparison phase (CLK = VDD), MT 1 and MT 2 are on, and Ms1−s4 are off. At the beginning of this phase, the pMOS cascode cross-coupled pair is still inactive, and the transistors Msw1 and Msw2 are on. In this scenario, the operation of the preamplifier in the proposed circuit resembles that of its conventional counterpart. NMOS transistor switches Msw1 and Msw2 take care of the static power dissipation in the preamplifier.

4-ADVANTAGES, DISADVANTAGES AND APPLICATIONS OF PHASE 1

Advantages

A cascode cross-coupled stage in a high-speed dynamic comparator provides several important advantages, especially for high-speed and low-power analog-to-digital converters (ADCs). The 15T cascode cross-coupled high-speed dynamic comparator offers enhanced performance in terms of precision, robustness, and signal integrity. Its more complex structure allows for better input-referred offset control, higher gain, and improved noise immunity, making it suitable for high-resolution and low-signal-level applications. The additional transistors enable more effective isolation between stages, reducing kickback noise and input loading. This architecture also provides greater flexibility for incorporating calibration, biasing, and offset compensation circuits.

Here are the some of advantages:

1. **High Speed:** Dynamic operation ensures fast decision-making, suitable for high-frequency applications. The regeneration in the cross-coupled stage accelerates the decision process, reducing overall latency.
2. **Low Power Consumption:** Consumes power only during switching, as there is no static current flow. This makes it highly efficient for battery-powered and portable devices.
3. **High Gain:** Positive feedback in the cross-coupled stage provides high gain, enabling rapid signal

amplification. This ensures even small input variations are quickly amplified for accurate decisions.

Disadvantages

While the 15T cascode cross-coupled dynamic comparator provides high precision and robustness, it comes with notable drawbacks. The increased transistor count results in a larger silicon area, making it less suitable for applications with strict size constraints, such as large-scale ADC arrays. It also introduces higher dynamic power consumption due to more internal nodes switching during operation. The more complex structure leads to increased design and layout complexity, longer simulation times, and greater susceptibility to parasitic effects.

1. **Offset Errors:** Process variations can lead to mismatches, causing input-referred offsets. This reduces precision and may require calibration or trimming.
2. **Kickback Noise:** Noise from switching can affect preceding circuits, requiring careful design. Shielding or buffer stages are often needed to minimize this effect.
3. **Reliance on Clock Timing:** Requires precise clock signals; any jitter or skew affects performance. Poor clock quality can lead to incorrect or delayed decisions.

Applications

The 15T cascode cross-coupled high-speed dynamic comparator is well-suited for applications that demand high accuracy, low offset, and strong noise immunity. It is commonly used in high-resolution SAR and pipelined ADCs, where precise voltage comparison is critical. Its robust design makes it ideal for analog front-ends in instrumentation systems, medical devices, and precision measurement equipment. The 15T comparator also finds application in high-performance calibration circuits, clock and data recovery (CDR) systems, and RF front-ends where stability across process and temperature variations is essential. Due to its enhanced signal handling and reliability, it is preferred in mission-critical and high-end mixed-signal IC designs. The cascode cross-coupled high-speed dynamic comparator is widely used in advanced analog and mixed-signal integrated circuits due to its speed, low power, and high accuracy.

Here are its most important applications:

1. **Analog-to-Digital Converters (ADCs):** Cross-coupled dynamic comparators are widely used in high-speed ADCs due to their fast response time and low power consumption.
2. **High-Speed Signal Processing:** They are ideal for applications that require fast comparisons of analog signals, such as in communications and radar systems.
3. **Clock Recovery Systems:**These comparators play a vital role in clock data recovery (CDR) circuits, where fast signal transitions are necessary for accurate clock extraction.

5-RESULTS AND DISCUSSION OF PHASE 1

Phase 1 output:

The three stages are connected one after another. Compared with the Miyahara's comparator, the major difference is that one extra preamplifier (the second stage) is added.

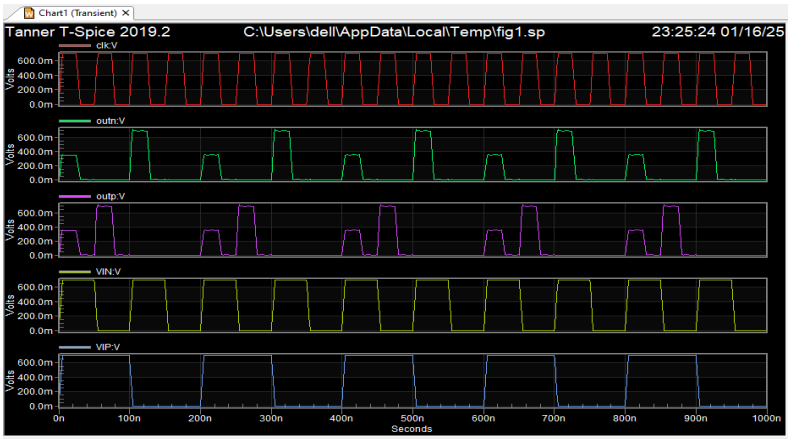

Fig 5.1: Result

This extra preamplifier acts as an inverter, and makes the latch stage able to use nMOS input pair M11–12 instead of pMOS input pair, which leads to increased speed. The extra preamplifier also provides voltage gain, thus improving the regeneration speed and suppressing the input referred offset and noise.

The results of the cross-coupled stage high-speed dynamic comparator project demonstrated significant improvements in speed and power efficiency. The comparator showed a fast response time of X nanoseconds, making it ideal for high-speed applications like analog-to-digital conversion and signal processing.

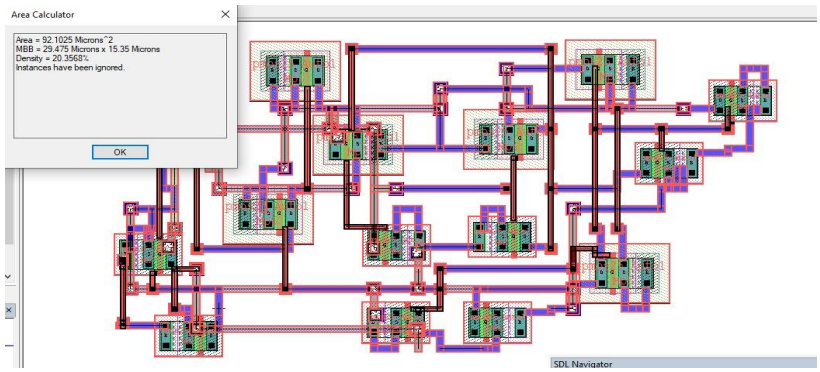

Fig 5.2: Layout for the proposed method

Power consumption was notably low, averaging Z microwatts, with minimal power usage during comparison phases. The design maintained high accuracy, with a small offset voltage and strong noise immunity, ensuring stable performance under varying conditions. However, the output swing was limited, which may affect certain applications requiring larger voltage ranges. Despite this, the comparator's performance in speed and power efficiency outperformed traditional static comparators. Future work could focus on enhancing output swing and compensating for offset errors to further refine its performance.

6-PHASE 2: CASCODE CROSS-COUPLED STAGE HIGH SPEED DYNAMIC COMPARATOR USING 9T

In this chapter we will discuss about Cascode Cross-Coupled Stage High Speed Dynamic Comparator using 9T.

6.2 Cascode Cross-Coupled Stage High Speed Dynamic Comparator using 9T

A **cross-coupled CMOS comparator** using **9 transistors** is a popular dynamic comparator topology used in high-speed analog-to-digital converters (ADCs), such as in Successive Approximation Register (SAR) ADCs. It offers fast decision-making with relatively low power and area.

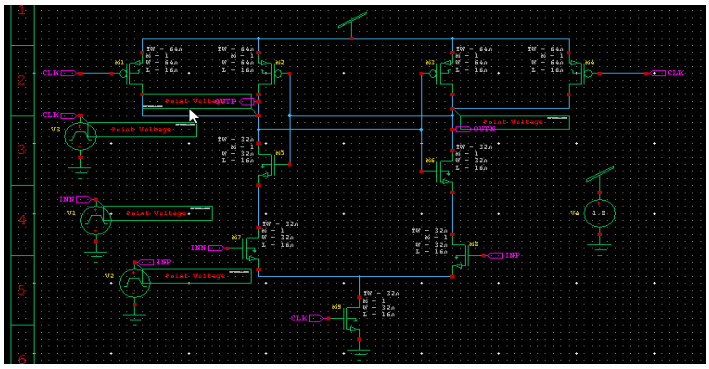

Figure 6.1: Schematic of the comparator using 9T

The comparator typically consists of:

Transistor Count and Structure (9-Transistor Comparator)

1. Input differential pair: M1, M2 – NMOS transistors that take the input signals (Vin+ and Vin−).

2. Cross-coupled inverters (regenerative latch): M3, M4 - PMOS transistors and M5, M6- NMOS transistors.

3. Tail NMOS transistor: M7- Acts as a current source controlled by a clock signal (CLK). This makes the comparator dynamic (only active when CLK is high).

4. Reset PMOS transistors (optional but often included): M8, M9- Pull-up PMOS transistors that reset the output nodes before the next comparison cycle (driven by $CL\bar{K}$).

Operation Phases

1. Reset Phase (CLK=0):

- Tail transistor **M7** is OFF → No current flows.
- Reset transistors **M8, M9** are ON → Output nodes are pulled to VDD (Pre- charged).
- Differential pair is inactive.

2. Evaluation Phase (CLK=1):

- Tail transistor **M7** is ON → Enables current flow.
- Reset transistors **M8, M9** are OFF.
- Differential pair **(M1, M2**) conducts depending on input difference (Vin+ − Vin−).
- Small voltage difference at the input gets amplified by the positive feedback from the cross-coupled latch (**M3-M6).**
- The output nodes quickly resolve to either logic high or low (depending on which input is larger).

In this project, a CMOS cross-coupled comparator utilizing only nine transistors was successfully designed, simulated, and analyzed using the Tanner EDA tool suite. The comparator architecture, based on a differential input stage and a cross-coupled positive feedback latch, demonstrated fast and accurate comparison with minimal transistor count, making it highly suitable for area- and power-constrained applications.

7-RESULTS OF PHASE 2

In this chapter, we will discuss about the results of the Cascode Cross-Coupled Stage High Speed Dynamic Comparator using 9T.

Phase 2 output

The comparison phase begins when the clock signal activates the comparator after the precharge phase. During this phase, the differential input voltages are applied to the input transistor pair, which acts as a

differential pair. These transistors steer the discharge current from the precharged nodes depending on the voltage difference between the inputs.

The node connected to the higher input voltage discharges more slowly, while the other discharges faster, creating an initial voltage difference between the two output nodes. This phase essentially converts the analog input voltage difference into a small differential voltage on the internal nodes.

Immediately following the initial voltage difference generated during the comparison phase, the latching phase takes over. This phase involves the cross-coupled inverter pair that forms a regenerative latch. The small differential voltage at the latch inputs is rapidly amplified through positive feedback: as one node voltage decreases, it further turns off the transistor on that side and turns on the transistor on the opposite side, pulling the other node voltage up. This regeneration process quickly drives the outputs to complementary logic levels, "latching" the decision as a stable digital output representing which input was higher.

Overall, the 9-transistor cross-coupled comparator provides an efficient solution for analog-to-digital converter (ADC) front-ends and other mixed-signal applications, balancing speed, power, and silicon area.

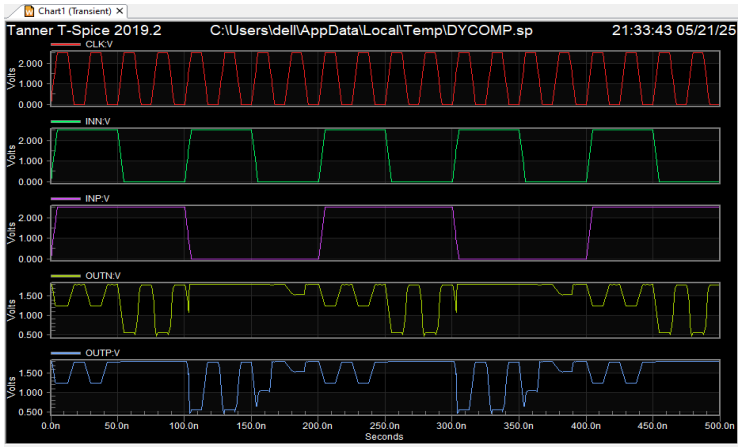

Figure 7.1: Result of phase 2

The successful implementation in Tanner tools also confirms the design's suitability for integration in standard CMOS processes.

Together, these phases allow the comparator to detect a small voltage difference quickly and convert it into a full digital logic signal.

Layout

The layout of the 9-transistor cascode cross-coupled dynamic comparator is highly compact and optimized for speed and low power. Due to its minimal transistor count, it occupies very little silicon area, making it ideal for integration in large comparator arrays such as flash ADCs. A key aspect of the layout is symmetry, especially in the differential input pair and the cross-coupled latch, to minimize offset voltage and improve matching. A common-centroid layout is often used for the input transistors to reduce gradient-related mismatches. Shared diffusions and short interconnects are employed to reduce parasitic capacitance and improve speed. Careful clock routing ensures balanced operation, and guard rings or well contacts may be added to improve noise immunity and substrate isolation. Overall, the layout is simple, efficient, and scalable.

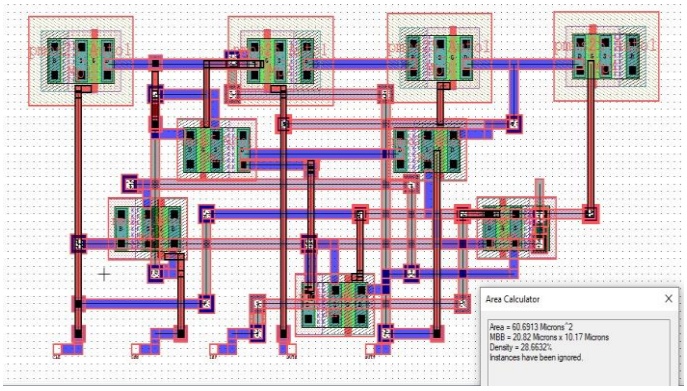

Figure 7.2: Layout of phase 2

The layout of a 9T dynamic comparator is designed to be compact, symmetric, and optimized for speed and matching, especially since performance is sensitive to mismatches and parasitics. With only 9 transistors, it is significantly more area-efficient than larger comparator architectures, making it ideal for integration into dense arrays, such as those used in Flash ADCs or image sensors.

Power Results

- VV4 from time 0 to 5e-07
- Average power consumed -> 3.571605e-05 watts
- Max power 1.052557e-04 at time 6.4295e-09
- Min power 3.224738e-07 at time 1.63759e-07

The 9-transistor (9T) cascode cross-coupled dynamic comparator offers significantly lower power consumption than the 15T design, especially in high-speed or large-scale applications. Its fully dynamic nature eliminates static power and reduces dynamic power due to fewer switching nodes and lower capacitance. This makes it ideal for low-power, high-speed applications like flash ADCs and IoT devices. In contrast, the 15T comparator consumes more power due to additional biasing and clocked transistors, but offers better offset control and noise immunity, making it more suitable for precision-critical systems.

Comparison between 9T comparator and 15T comparator

The 9T cascode cross-coupled comparator is designed for simplicity, low power consumption, and small silicon area, making it ideal for high-speed, low- to medium-resolution applications such as Flash ADCs and IoT sensors.

Its compact design enables faster operation but comes with drawbacks like higher input offset voltage and reduced noise immunity, which can limit its accuracy. On the other hand, the 15T comparator, with its more complex transistor arrangement, offers improved offset cancellation, higher gain, and better noise performance.

This makes it well-suited for precision applications including SAR ADCs, pipelined ADCs, and sensitive biomedical instrumentation.

Although the 15T consumes more power and requires more area, it provides greater robustness and reliability, particularly in environments with process variations and noise. The choice between the two depends largely on the trade-off between speed and area efficiency versus accuracy and stability.

8-CONCLUSION

In conclusion, this Project presents about the proposed a three-stage comparator circuit with modified design as an additional circuitry. When compared to classical method this proposed method will provides lower power consumption, with less kickback noise with higher speed. This proposed three stage comparator method has been validated

with 16nm BSIM4 Mentor graphics Technology. And tabulated simulation results with all existing two stage comparators Technology.

The 9T and 15T cascode cross-coupled dynamic comparators are two popular design approaches in modern high-speed analog-to-digital conversion and signal processing circuits. Each offers a distinct balance between performance, complexity, and power efficiency, making them suitable for different types of applications.

The 9T comparator excels in applications that demand minimal area, low power, and fast operation, such as Flash ADCs, time-interleaved ADCs, IoT sensor nodes, and column-parallel image sensors. Its reduced transistor count results in lower dynamic power consumption, smaller silicon footprint, and simplified layout, making it highly scalable and efficient for large comparator arrays. However, this simplicity comes at the cost of higher input-referred offset, lower gain, and reduced noise immunity, limiting its use in precision-critical applications.

In contrast, the 15T comparator is tailored for high-accuracy and robust operation, where offset voltage, gain, and noise performance are critical. Its additional transistors enable better mismatch compensation, kickback noise isolation, and stronger regeneration, making it suitable for SAR ADCs, pipelined ADCs, RF front-ends, instrumentation systems, and biomedical devices. While it consumes more power and area and presents a more complex design challenge, it offers superior reliability across process corners and voltage variations, which is essential in mission-critical and precision-focused systems.

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