AN ON-CHIP BUS TRACER WITH REAL TIME AND BUS TRACKING SYSTEM WITH SOC

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ABSTRACT

A multiresolution AHB on-chip bus tracer named SYS-HMRBT (AHB multiresolution bus tracer) for versatile system-on-chip (SOC) debugging and monitoring. The bus tracer is capable of capturing the bus trace with different resolutions, all with efficient built-in compression mechanisms, so meet a diverse range of needs. In addition, it allows users to switch the retrace resolution dynamically so that appropriate resolution levels can be applied to different segments of the trace. On the other hand, SYS-HMRBT runs at 500 MHz and costs 42K gates in TSMC 0.13-µm technology, indicating that it is capable of real time tracing and is very small in modern SOC’s.

INTRODUCTION

The real time multiresolution AHB on-chip bus tracer, named SYS-HMRBT (AHB multiresolution bus tracer). The bus tracer adopts three trace compression mechanisms to achieve high trace compression ratio. It supports multiresolution tracing by capturing traces at different timing and signal abstraction levels. In addition, it provides the dynamic mode change feature to allow users to switch the resolution on the fly for different portions of the trace to match specific debugging/analysis needs. Given a trace memory of fixed size, the user can trade off between the granularity and trace length to make the most use of the trace memory. In addition, the bus tracer is capable of tracing signals before/after the event triggering, named pre-T/post-T tracing, respectively.

There are many research works related to the bus signal compression. We characterize the bus signals into three categories: program address, data address/data and control signals. We then review appropriate compression techniques for each category. For program addresses, since they are mostly sequential, a straightforward way is to discard the continuous instruction addresses and retain only the discontinuous ones, so called branch/target filtering. This approach has been used in some commercial traders, such as the TC1775 trade module in Tricore and ARM’s Embedded trace Macrocell.
A main component of transport information services is predicting the arrival times of the next bus and providing this information to the public via various media. Due to the different operational conditions, the technologies used for arrival time estimation in transit modes such as rail systems can not directly be transferred to fixed route bus services. Rail transit is a well-controlled mode; vehicles have few external factors interfering with their progress and their locations. Real time bus tracking systems are a combination of the installation of a location-aware transmitter on a bus plus purpose-designed computer software to collect the data and enable its storage, display and analysis. Modern bus tracking systems commonly use GPS technology for locating the bus, but other types of location technology can also be used. Bus real time information can be viewed on electronic maps and diagrams via a web browser or using specialized software, urban public transit authorities are an increasingly common user of bus tracking systems, particularly in large cities. By real time bus tracking systems, bus services provide on the fly information to their users, including the current locations of buses and the predicted arrival times at bus stops. Urban transit agencies use the technology for a number of other purposes, including monitoring schedule adherence of buses in service. In order to improve services, ads well as providing real time information, real time bus tracking systems can build up an archive of data that can be analyzed and mined for information to show the behavior of the transport system over time, indicating common problems such as vehicle bunching and delays due to congestion. In a joint project between NUI Maynooth and Blackpool Transport, a real time bus tracking system has been built allowing the operator to assess and improve the quality of their public service. Knowledge of the vehicle location enables fleets of vehicles to be tracked and managed. Various real-time bus tracking systems use different techniques to determine a vehicle’s location, usually in terms of distance to a particular bus stop on the route. In , the timestamp of GPS data points at or near a bus stop are considered as arrival times at the bus stops. Suggests creating artificial “sign-posts” inside the computer software.

The OV10630 and OV10635 system-on-chip (SoC) sensors raise the bar in automotive imaging by combining megapixel resolution with color HDR in a 1/27-inch optical format. The AECC0100 qualified OV10630 and OV10635 come with a full set of automatic controls and an image processing pipeline for display and sensing applications. Ideally suited for wide field of view and multi-camera applications, the FOv10630 AND OV10635 also incorporate special features and output formats for automotive machine vision applications, with its proprietary capability to simultaneously deliver high image quality and superior scene information, the FOv10630 and OV10635 are designed functions concurrently. The two sensors are similar in functionality and performance but are integrated in different packages, giving customers greater flexibility.

The sensors are built on a 4,2-micron OmniPixel13-HS® pixel, enabling best-in-class low light sensitivity of 3,65 V/lux-sec to capture detail rich, high definition color video in any environment. Using a proprietary new high dynamic range (HDR) concept and processing technology, these automotive sensors deliver excellent scene reproduction in the most demanding lighting conditions, achieving a dynamic range up to 115 dB in color and black-and-white. The OV10630 and OV10635 not only have the ability to accurately reproduce
high-contrast scenes, but also employs auto dynamic range control to adjust to changing lighting and scene conditions to produce a clear, detailed and low-noise color image in any automotive situation. A proprietary approach to generating HDR images also dramatically reduces or eliminates many typical HDR image sensor artifacts such as motion ghost artifacts and other unwanted effects.

The OV10630 and OV10635 offer all required automatic image control functions, including automatic exposure control, automatic white balance, automatic black level calibration, as well as defective pixel correction, gamma correction and lens shading correction. The sensors support a digital video parallel port, and provide full-framed or windowed 10-or 8 bit YUV and 10 to 18 bit combined HDR RAW output format with complete user control over formatting and output data transfer. Camera functions are programmable through the serial camera control bus (SCCB) interface. Additional features include a horizontal and vertical windowing capability, external frame sync capability, 50/60 Hz flicker cancellation and low power consumption.

APPLICATIONS

Single Core on extended 6502 bus:

The following figure represents a block diagram of a generic simple platform based on a single 6502EX core connected to memory and to peripherals by means of extended 6502 bus. Basically, the extended 6502 bus implies larger memory space addressability (up to 32bit) and larger data memory support (8bit or 32bit). The extended 6502 bus contains also additional control signals not existing in the legacy bus protocol, they are not shown in the following schemes.

In this example the code/data bus is limited to 8bit.

![Figure 1: Single Core platform on extended 6502 bus](image)

The orange bus represents the 6502EX program fetch and data access bus. Memories are connected to this bus. A DMA facilitates data moving between the SPI and the memory. The memory sub-system is built-up around a ROM and a synchronous RAM. The blue bus represents the 6502EX System Register bus to which the user can connect the programming registers of his peripherals without interfering with the main bus. The System Register bus becomes the configuration bus of the system. Still in this example, the System Register bus is connected to General Porpoise Register (GPIO) to be used to control the external world.
Single Core with Coprocessor on AHB bus:

In this example the 6502EX is connected to a coprocessor through the System Register bus. The coprocessor in this case has local dedicated memories. The 6502EX main bus and the System Register bus are wrapped respectively on AHB protocol and APB protocol. The exposed AHB bus gives access to the huge number of legacy AHB peripherals available on the market. The exposed APB bus is used as configuration bus to program AHB peripherals.

In this case the 6502EX main bus is 32bit large to speed up data access, enabling implementation of 32bit software stack for faster subroutine calls management.

![Figure 2: Single Core with Coprocessor on AHB bus](image)

Twin Core with Coprocessor on extended 6502 bus:

This is an interesting example showing a system composed by two 6502EX cores and two coprocessors realizing a low cost eyes tracking system.

![Figure 3: Eyes Tracking System](image)

The TCB block (Twin Core Bus) gives the possibility to easily connect the two 6502EX cores to the same memories and to the same peripherals without making the design complex. In fact, TCB exploits a time-division bus sharing principle that makes practically transparent to the user the management of the two cores running in parallel. Thanks to this technique the timing of the application is always predictable for both the threads (particularly suggested for
strong real time application). The bus clock (ckb) is supplied to TCB that derives two slower clocks (divided by two), ck1 and ck2, which are supplied respectively to core1 and core2. Pay attention that ck1 and ck2 are in counter-phase. This way, each core always takes its bus slot to make code/data accesses without interfering with the other.

![Figure 4: bus and cores clock phases](image)

Thanks to this clock scheme, the two cores can access the same memory without clock penalties (wait state due to arbitration). The Camera interface connects the camera to the system in order to transfer the frames of the scene that will be processed by the eyes tracking algorithm running into the two cores and into the two coprocessors. Finally, the USB interface transfers the processed data externally to the host system that will take the proper action (e.g. a PC that moves the cursor on the monitor when the user watches the monitor and moves the eyes). This MIPS demanding application is enabled thanks to a dedicated coprocessor (this application uses two of them connected to two different 6502EX) called GAZE. GAZE is a sophisticated coprocessor implementing an optimized state of the art real-time eyes tracking algorithm that makes possible silicon low cost implementation without performance compromise.

The software watches the GPS data and sets a flag when the bus has moved close enough to an identified location. In, the arrival of the vehicle at the bus stop is assumed if a single GPS positional update for that vehicle is detected inside a predefined circular proximity zone and the detected inside a predefined circular proximity zone and the detected speed is lower than a predefined upper threshold. The reason for this condition is due to the nature of streamed GPS positional data. A more precise condition would be if there are two consecutively detected GPS positional updates within a defined proximity to the bus stop with a speed of 0km/h. Are tracked as a matter of course for safety, signaling and other reasons. Real-time bus locations can not be determined or estimated as accurately without external sensors, so bus location or arrival time information often has a degree of uncertainty. This uncertainty is likely to be higher due to the presence of a number of factors such as traffic congestion and intersection delays, and weather conditions.

**CONCLUSION**

An on-chip bus tracer SYS-HMRBT for the development, integration, debugging, monitoring, and tuning of AHB-based SOC’s. it is attached to the on-chip AHB bus and is capable of capturing and compressing in real time the bus traces with five modes of resolution. These modes could be dynamically switched while tracing. The bus tracer also supports both directions of traces: pre-T trace and post-T trace. In addition, a graphical user interface, running on a host PC, has been developed to configure the bus tracer and analyze the captured traces. With the aforementioned features, SYS-HMRBT supports a diverse range.
of design/debugging/monitoring activates, including module development, chip integration, hardware/software integration and debugging, system behavior monitoring, system performance/power analysis and optimization, etc.

**SIMULATION RESULTS**

**MODE FC**

Simulation results of Mode FC

**MODE FT**

Simulation results of Mode FT

**MODE BC**

Simulation results of Mode BC

**MODE BT**

Simulation results of Mode BT

**REFERENCES**

[1] Lakshmanan V. Bus travel time prediction using GPS data proceeding of map India.


