IMPLEMENTATION OF LC RESONANT CLOCK DISTRIBUTION NETWORKS USING LOW SWING DIFFERENTIAL CONDITIONAL CAPTURING FLIP-FLOP

BK Siva Keerthi*1, H Devanna2

1M.Tech Student, Dept of ECE, St. Johns College of Engineering and Technology, Yerrakota, Yemmiganur, Kurnool (A.P), India.
2Assoc Prof, Dept of ECE, St. Johns College of Engineering and Technology, Yerrakota, Yemmiganur, Kurnool (A.P), India.

ABSTRACT
Since delay buffers are unit accessed consecutive, it adopts a ring-counter addressing theme. Within the ring counter, double-edge-triggered (DET) flip-flops square measure used to scale back the operative frequency by 0.5 and therefore the C-element gated-clock strategy is planned within the existing Paper, a unique gated-clock-driver tree is then applied to additional cut back the activity on the clock distribution network. Moreover, the gated-driver-tree plan is additionally utilized within the input and output ports of the memory block to decrease their loading, therefore saving even additional power. Multimedia system and communication devices have skilled explosive growth recently. Longer battery life is one in every of the crucial factors within the widespread success of those product. As such, low-power circuit style for multimedia system and wireless communication applications has become important. During this paper we tend to square measure reaching to style a brand new low power edge triggered flip-flop for the appliance of the gated driver tree, low power buffer taken from the present papers.

Keywords: Flip-flop, Low Power Buffer, Gated Driver Tree, DSCH, Micro wind.

1. INTRODUCTION
In several such merchandise, delay buffers (line buffers, delay lines) conjure a big portion of their circuits. Such serial access memory is required in temporary storage of signals that ar being processed, e.g., delay of 1 line of video signals, delay of signals inside a quick Fourier rework (FFT) architectures, and delay of signals during a delay correlator. Currently, most circuits adopt static random access memory (SRAM) and some control addressing logic to implement delay buffers. For smaller-length delay buffers, register are often used instead, the previous approach is convenient since SRAM compilers ar pronto offered and that they ar optimized to come up with memory modules with low power consumption and high operation speed with a compact cell size. The latter approach is additionally convenient since register are often simply synthesized, although it should consume abundant power thanks to redundant information movement.

To effectively scale back dynamic power, hardware designers should perceive a mess of clock-gating transformations and have the sensible expertise to grasp once they ought to be applied. The exchange between power reduction and verification price isn't continually clear thus designers tend to take care, Clock-gating altogether shapes and sizes. Power has become a primary thought throughout hardware style. Dynamic power will contribute up to five hundredth of the overall power dissipation. Clock-gating is that the most typical RTL optimization for reducing dynamic power. Effective clock-gating implementation needs skillful application and comprehensive verification. There’s a colossal array of clock-gating techniques offered to designers. Clearly not all of those ar equal once it involves reducing change activity. Several transformations ar easy, whereas others ar extremely guarded, proprietary algorithms. Most clock-gating is finished at the Register Transfer Level (RTL). RTL clock-gating algorithms are often sorted into 3 categories: system-level, serial and combinable. System-level clock-gating stops the clock for a whole block, effectively disabling all practicality. On the contrary, combinable and serial clock-gating by selection suspend duration whereas the block continues to provide output. Combinable clock-gating could be a easy substitution to the RTL code. It reduces power by disabling the clock
in registers once the output isn't ever-changing. Opportunities to insert combinable clock-gating are often found by longing for conditional assignments within the code. Clock-gating logic is substituted once code like "if (cond) out <= in" is gift. Combinable clock-gating is currently a feature within the RTL compilers. Power aware synthesis tools establish RTL committal to writing patterns and build the acceptable substitution. Hardware designers solely have to be compelled to perceive some easy RTL committal to writing tips to realize the advantages of combinable clock-gating.

Since combinable clock gated flops maintain a 1 to 1 state mapping with the first RTL, combinatory Equivalence Checking Tools will be used for practical verification. This makes verification straightforward to setup and comprehensive. On the opposite hand as a result of shift activity is eliminated only information isn't dynamical, the particular power savings is restricted. In typical styles, combinatory clock-gating will cut back dynamic power by regarding 5-to-10%. Sequent clock-gating alters the RTL micro-architecture while not touching style functionally. Power is optimized by distinctive unused computations, information dependent functions and don't-care cycles within the original code. There are a unit many varieties of sequent clock-gating transformations. Distinctive opportunities for sequent clock-gating is troublesome, requiring sequent analysis. One example of a sequent improvement is popping off resultant pipeline stages supported a propagated valid logic, this transformation is smart provided that the data path is multiple bits wide.

Sequential clock-gating could be a multi-cycle improvement with multiple implementation tradeoffs and RTL modifications. Consequently there's a larger demand on practical verification resources. On the opposite hand serial clock-gating will save vital power, generally reducing switch activity by 15-to-25% on a given block.

2. STANDARD CONDITIONAL GATED DRIVER TREE STYLE

Although some power is so saved by gating the clock signal in inactive blocks, the additional R–S flip-flops still function loading of the clock signal and demand over necessary clock power. We have a tendency to propose to
exchange the R–S flip-flop by a C-element and to use tree-structured clock drivers with gating thus on greatly scale back the loading on active clock drivers, to boot, DET flip-flops area unit wont to scale back the clock rate to half and therefore additionally scale back the ability consumption on the clock signal. The projected ring counter with gradable clock gating and also the management logic.

![Gated Driver Tree Architecture](image1)

Each block contains one C-element to manage the delivery of the local clock signal $\text{CLK}_{ij}$ to the DET flip-flops, and solely the CKE signals on the path passing the worldwide clock supply to the local clock signal area unit active. The “gate” signal CKE may be derived from the output of the DET flip-flops within the ring counter. The C-element is a necessary part in asynchronous circuits for acknowledgement. One in all its implementation.

3. LOW SWING DOUBLE-EDGE TRIGGERED FEEDBACK FLIP-FLOP

The power consumption of the systems is a critically important parameter in modern VLSI circuits especially for low power applications and, hence, the power optimization techniques should be applied at different levels of the digital design. One of these techniques is to use low power logic styles which should be used in design of latches and flip-flops (FF’s) which are among the components widely used in digital systems [1,2]. There are other concerns in the design of DFF’s such as $T_{\text{clk}}$ (delay from $\text{clk}$ to output of FF) and $C_{\text{clk}}$ (the load capacitance of the clock) which are also should be minimized to maximize the FF performance.

Resonant duration permits the generation of clock signals with reduced power consumption. The normal approach for LC resonant CDNs is to use the LC tank to drive the world clock distribution whereas the local square clock is being delivered through standard buffers. However, around sixty six of clock power is being dissipated within the last buffer stage driving the flip-flops resulting in minor power savings in LC globally-resonant locally-square CDNs. Therefore to realize most power savings, the LC tank ought to drive the whole clock network (both world and local) while not exploitation intermediate buffers. This would require coming up with, modifying and understanding flip-flop performance with the curved clock signal generated in LC resonant networks.

![Existing low-swing LC resonant clocking](image2)

4. OUR PROPOSED LOW POWER CLOCKED PASS TRANSISTOR FLIP-FLOP DESIGN

By using the Pass Transistor Logic family idea we are designing this circuit as well as by using the pass transistor logic we are using only one clocking transistor so it will be consuming only less power in the clock network of the Flip flop when compared to all other circuits. As well as we are having only 6 Transistors excluding the not gates also. So we will be having much reduced power and area when compared to the other two designs. At the same time due to the reduced no of transistor count we can reduce the delay oriented things
also. Thus we are reducing the overall switching delay and power, area consumption. So this circuit will be acting as good sequential elements when compared to other flip-flop design.

Fig 3: Our Proposed Low Power Clocked Pass Transistor flip-flop

Fig 4: Waveform Output of the Proposed Low Power Clocked Pass Transistor flip-flop

The graph represents the input & output characteristics of our proposed system from that we can clearly understand how it works as negative edge triggered flip-flop. There is some nano seconds delay is there even though it’s a negligible amount only. Those delays can be further reduced by reducing the sizes of the transistor we are using in this circuit. Or by reducing the nano meter technology also we can reduce the constraints. The Layout design of the proposed new flip-flop is shown in the figure 6 the area of that is mentioned at the downside of the layout. The Power consumption characteristics also mentioned below in figure 5.

Fig 5: Layout of the LCPTFF proposed design
Thus the Our Proposed Low Power Clocked Pass Transistor flip-flop design shows much less power & Area constraints than the Existing two Flip-Flop designs. As well as the Proposed design will be having very less clock delay when compared to all other circuits. So it can be used in all the future sequential elements for high speed low SOC’c manufacturing.

5. CONCLUSION

In this Paper we tend to projecteda replacementduration System based mostly D flip flop stylethatis known asas Low Power Clocked Pass semiconductor device flip-flop style. The projected system shows Power improvement than the prevailing Double Edge Triggered Flip-Flop D Flip-Flop associate degree it shows an improvement of in space constraints additionally. Therefore our projected system has less power and space constraints similarlybecause it has a awfully low power duration system which is able to result in improvement within the case implementation in future mobile devices. In future it are oftenterrribly inappropriate for System on Chip SOC applications which is able to lead U.S.A. to a brighter tomorrow with low power consumption. This will be a lot of inappropriate for application of battery oriented operation for fewer power and space. In future we will add another escape reduction techniques and use the power are oftenmore reduced.

REFERENCES