A CASCADED H-BRIDGE AND NOVEL MULTILEVEL INVERTER TOPOLOGY FOR INDUCTION MOTOR DRIVE

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ABSTRACT
The poor quality of voltage and current of a conventional inverter fed induction machine is due to the presence of harmonics and hence there is significant level of energy losses. The nine level inverter is used to reduce the harmonics. The inverters with a large number of steps can generate high quality voltage waveforms. The concept of multilevel inverters, introduced about 20 years ago entails performing power conversion in multiple voltage steps to obtain improved power quality, lower switching losses, better electromagnetic compatibility, and higher voltage capability. The benefits are especially clear for medium-voltage drives in industrial applications and are being considered for future naval ship propulsion systems. The application of pulse width-modulated (PWM) voltages using two-level high-voltage inverters to a squirrel-cage induction motor (SQuIM) can cause heating of rotor shaft, voltage spike across the motor terminals, etc. The increase in the number of steps of the motor voltage and hence decreasing the \( \frac{dv}{dt} \) applied to the machine terminals can be a solution to this problem. The existing topologies that generate this multistep voltage include cascading of a number of single-phase inverters or use of higher order multilevel inverters. In this paper, a topology with series connection of three-phase three-level inverters is proposed, which addresses the problems of medium-voltage drives.

Keywords: Medium-voltage ac drives, multilevel converter topologies.

I. INTRODUCTION
The necessity of increasing the power quality enhancement in industry has sustained the continuous development of multilevel inverters due to high efficiency with low switching frequency control method. The multilevel inverters improve the AC power quality by performing the power conversion in small voltage steps resulted in lower harmonics. The output voltage on the AC side can take several discrete levels of equal magnitude. The harmonic content of this output voltage waveform is greatly reduced, a smaller filter size and a lower EMI, if compared with a two level voltage waveform. Several topologies for multi-level inverters have been proposed over the years the most popular being the diode clamped, flying capacitor and cascaded H-bridge structures. One aspect which sets the cascaded H-bridge apart from other multi-level inverters is the capability of utilizing different DC voltages on the individual H-bridge cells which results in splitting the power conversion amongst higher-voltage lower-frequency and lower-voltage higher frequency inverters.
With the rapid development of socioeconomic and energy demand, there are more and more concerns on how to secure a clean sustainable and economic energy supply for the future. This leads to demands on building high power converters with more flexible, intelligent control and management of power flows in order to secure a unified stable converter, which interlinks different loads or power sources. Following that trend, an advanced power converter without line frequency transformer was proposed. Because of the cascaded H-bridge multilevel topology adopted in its rectifier stage, this advanced high power converter could be used between two different high-voltage systems without line-frequency transformer.

The cascaded multilevel converter consists on series connected H-bridge units. Each H-bridge provides three voltage levels (+udc, 0, -udc). The number of levels that is possible to obtain at the output is m=2N+1, being N the number of H-bridges connected in series. The use of cascaded H-bridge structure allows reduced stress for semiconductor devices greatly reducing failures and significantly extending the life of the converter, allowing the use of optimized electrical machines and smaller filters and, consequently, cost reductions. Nowadays, the advantages of cascaded H-bridge converter are well recognized for high power, medium voltage applications. The control of such a rectifier stage is a complex task characterized by a threefold goal to satisfy AC-side unity power factor, to obtain satisfactory load voltage regulation and to reduce harmonics of system in the AC-side. In addition, it requires the balancing of the DC-link voltage for all the H-bridges to ensure high voltage application.

An alternate method of cascading inverters involves series connection of two, three-phase inverters through the neutral point of the load. Past research has shown this concept for cascading two-level inverters and multi-level inverters. An advantage of this approach is that isolated sources are not required for each phase. It should be noted that cascaded inverter systems can be considered from a number of different viewpoints. Considering the cascaded inverter to be one unit, it can be seen that a higher number of voltage levels are available for a given number of semiconductor devices. Multilevel power inverters employ power semiconductor switches in the inverter to select one or more of multiple dc voltage sources to create staircase voltage waveform at the inverter output. Capacitors batteries or renewable energy voltage sources can be used as a DC voltage sources. The control of the power switches permits the addition of the multiple DC sources in order to achieve desired staircase waveform at the high power output. This paper highlights sinusoidal PWM based cascaded multilevel schemes is discussed. This scheme does not require any modification in the carrier or modulating signal. It has advantage or superiority over other previous works.
Induction motors are widely used in industries because it has offer lot of advantages. Cascaded multilevel inverter output is fed to the induction motor to verify the basic performance of the inverters like voltage fluctuation, frequency variation, etc. Since the induction motor is treated as the load to the multilevel inverter, any variation in the performance of multilevel inverter reflects on the performance of motor. The proposed method of an eleven-level cascaded multilevel inverter fed to induction motor drive performance is verified through simulation.

II. PROPOSED CONVERTER TOPOLOGY

The proposed general configuration of “n” number of three level inverters connected in series is shown in Fig. 1. Each inverter module is a three-phase NPC three-level inverter. At the output stage, transformers are used to have the series connection of three-level inverters, as shown in Fig. 1. If “Vdc” is the dc-bus voltage of each inverter module, then “α” is the turns ratio of each transformer and “n” is the number of inverter modules then for sine PWM (SPWM) strategy; the motor rms phase voltage ($V_{\text{ph, motor}}$) can be expressed as follows

\[
R_{\text{rms}} = V_{\text{dc}} \alpha \frac{m}{\sqrt{2}}
\]

Where $m$ is the modulation index of the inverter topology defined as follows

\[
m = \frac{\text{Peak of } V_{\text{ph, inverter}}}{V_{\text{peak}}}
\]

$V_{\text{ph, inverter}}$ is the total phase voltage reference of the inverter topology. For the given peak of $V_{\text{Ph, motor}}$, peak of $V_{\text{ph, inverter}}$ can be computed as follows

\[
\text{Peak of } V_{\text{ph, inverter}} = \frac{\text{Peak of } V_{\text{Ph, motor}}}{\sqrt{3}}
\]

The generation of individual reference voltage signal of each inverter is discussed as follows.

The gate pulses for each three-level inverter module can be derived using two carrier signals. Thus, “n” numbers of such three-level inverter modules require “2n” number of carriers [10], [13]. The three-phase voltage reference signals are then compared with these carrier waves to
produce the gate pulses for the inverters. For example, the carrier waves and the sinusoidal modulating voltage signal (SPWM technique) for R phase is shown in Fig. 2 for four series-connected three-level inverters. The carrier waves 1 and 1_(Fig. 2) with R-phase voltage reference controls the inverter module 1. Similarly, 2 2_, 3–3_, and 4–4_ carrier waves with R-phase voltage reference generate the gate pulses for the three-level inverter modules 2, 3, and 4, respectively. Thus, each inverter module produces the voltage proportional to a part of the reference phase voltage signals. It is important to note that no two three-level inverter modules switch simultaneously (Fig. 2). Thus, the maximum dv/dt rate of the output voltage of this topology is limited to that of a single three-level inverter module (Fig. 5). The references of each inverter are shown in Fig. 3. The corresponding output line voltages of each inverter are shown in Fig. 4. The four windings, one from each transformer, are connected in series and produced the net R-phase voltage, as shown in Fig. 5 Similarly, the other two phase voltages are generated.

Fig 1: Block diagram of three-phase three-level inverter modules connected in series driving an SQIM.

Fig 2: Carrier waves and the sinusoidal modulating voltage signal for R phase in SPWM technique
The line voltage spectra of individual inverters are shown in Fig. 4 for switching frequency of 2.5 kHz. These line voltages get added to produce the net phase voltage of the topology. The voltage spectra are expressed as a percentage of the maximum total fundamental (Vpeak) that can be produced by the topology.

\[ V_{\text{peak}} = \sqrt{2} \cdot V_{\text{nominal}} \]

or \( V_{\text{peak}} = 2078.5 \text{ V} \) for \( V_{\text{dc}} = 600 \text{ V}, n = 4, \alpha = 1, \) and \( m = 1 \) using (1). Hence, the spectra show the percentage share of the fundamental of each inverter module. These spectra also suggest that the line voltages of all these inverters contain additional small amount of the 5th-, 7th-, 11th-, 13th-, and higher order harmonics besides the normal switching harmonics. However, the net phase voltage and line voltage of this topology do not contain any of these harmonics, as suggested by the spectra shown in Fig. 5. These harmonics get canceled when the line voltages of the individual inverters are added by the transformers to produce the net phase voltages. The increased number of steps in the motor terminal voltage reduces the \( \frac{dv}{dt} \) as that compared with a conventional two-level inverter.

Fig 3: Four series connected Inverters Individual voltages
III. DYNAMIC MODEL OF INDUCTION MOTOR

The induction machine d-q or dynamic equivalent circuit is shown in Fig. 1 and 2. One of the most popular induction motor models derived from this equivalent circuit is Krause’s model detailed in [5]. According to his model, the modeling equations in flux linkage form are as follows:

\[
\frac{dF_{\psi}}{dt} = \omega_b \left[ v_{\psi} - \frac{\omega_a - \omega_s}{\omega_b} F_{\theta r} + \frac{R_s}{x_{\psi t}} \left( F_{\psi q} + F_{\psi r} \right) \right] \tag{1}
\]

\[
\frac{dF_{\psi t}}{dt} = \omega_b \left[ v_{\psi t} + \frac{\omega_a - \omega_s}{\omega_b} F_{\psi r} - \frac{R_s}{x_{\psi t}} \left( F_{\psi q} + F_{\psi r} \right) \right] \tag{2}
\]

\[
\frac{dF_{\psi r}}{dt} = \omega_b \left[ v_{\psi r} - \frac{\omega_a - \omega_s}{\omega_b} F_{\psi q} + \frac{R_s}{x_{\psi t}} \left( F_{\psi q} - F_{\psi r} \right) \right] \tag{3}
\]

\[
\frac{dF_{\theta r}}{dt} = \omega_b \left[ v_{\theta r} + \frac{\omega_a - \omega_s}{\omega_b} F_{\psi q} - \frac{R_s}{x_{\psi r}} \left( F_{\psi r} - F_{\theta r} \right) \right] \tag{4}
\]

\[
F_{\psi q} = x_{\psi t}^* \left[ F_{\psi q} + F_{\psi r} \right] \tag{5}
\]

\[
F_{\psi r} = x_{\psi r}^* \left[ F_{\psi q} + F_{\psi r} \right] \tag{6}
\]

\[
i_{\psi} = \frac{1}{x_{\psi t}} \left( F_{\psi r} - F_{\psi q} \right) \tag{7}
\]
For a squirrel cage induction machine, as in the case of this paper, \( v_{qr} \) and \( v_{dr} \) in (3) and (4) are set to zero. An induction machine model can be represented with five differential equations as shown. To solve these equations, they have to be rearranged in the state-space form. In this case, state-space form can be achieved by inserting (5) and (6) in (1–4) and collecting the similar terms together so that each state derivative is a function of only other state variables and model inputs. Then, the modeling equations (1-4) of a squirrel cage induction motor in state-space become

\[
\begin{align*}
\frac{di_q}{dt} &= -\frac{1}{\psi_q} (F_{d\phi q} - F_{m\phi}) \\
\frac{di_r}{dt} &= -\frac{1}{\psi_r} (F_{q\phi r} - F_{m\phi}) \\
\frac{d\theta}{dt} &= \frac{1}{\psi_b} (F_{d\phi q} - F_{q\phi r}) \\
I_s &= -I_I = J \left( \frac{2}{p} \right) \frac{d\omega}{dt}
\end{align*}
\]

where
- \( d \): direct axis.
- \( q \): quadrature axis.
- \( s \): stator variable.
- \( r \): rotor variable.
- \( F_{ij} \) is the flux linkage (\( i=q \) or \( d \) and \( j=s \) or \( r \)).
- \( v_{qs}, v_{ds} \): \( q \) and \( d \)-axis stator voltages.
- \( v_{qr}, v_{dr} \): \( q \) and \( d \)-axis rotor voltages.
- \( F_{m\phi q}, F_{m\phi r} \): \( q \) and \( d \)-axis magnetizing flux linkages.
- \( R_s \): stator resistance.
- \( R_r \): rotor resistance.
- \( X_{ls} \): stator leakage reactance (\( \omega L_s \)).
- \( X_{lr} \): rotor leakage reactance (\( \omega L_r \)).
- \( X_{ml} \): \( 1/\left( \frac{1}{X_s} + \frac{1}{X_b} + \frac{1}{X_r} \right) \).
- \( i_{qs}, i_{ds} \): \( q \) and \( d \)-axis stator currents.
- \( i_{qr}, i_{dr} \): \( q \) and \( d \)-axis rotor currents.
- \( p \): number of poles.
- \( J \): moment of inertia.
- \( T_s \): electrical output torque.
- \( T_L \) or \( T_I \): load torque.
- \( \omega_s \): stator angular electrical frequency.
- \( \omega_p \): motor angular electrical base frequency.
- \( \omega_r \): rotor angular electrical speed.
IV. MATLAB/SIMULINK MODEL & SIMULATION RESULTS

Here simulation is carried out for two cases. In case I conventional three phase three level induction motor is simulated and in case II proposed multilevel drive is simulated.

Fig 6 Matlab/Simulink Model of Convention IM Drive

Fig. 6 shows the Matlab/Simulink model of conventional three phase three level induction motor drive. It consists of front end rectifier followed by three phase inverter.

Fig 7: Three Level output

Fig. 7 shows the three level output of the conventional inverter. Her switching frequency is taken as 1050 hz.
Fig. 9 shows the block diagram of proposed series connected multilevel inverter fed induction motor drive. It consists of four inverters. Here we are using phase shifted carrier PWM.
Fig 10: Three Level output Inverter 1  
Fig 11: Three Level output Inverter 2  
Fig 12: Three Level output Inverter 3  
Fig 13: Three Level output Inverter 4  

Fig 10 to 13 shows the individual inverter outputs. From the figures it is clear that each output consists of only three levels.

Fig 14: Multilevel output  
Fig 15: Multilevel output three phase  

This waveform represents the output voltage of the three phase multilevel inverter.

Fig 16: Electromagnetic Torque and Speed curves of SQCIM
The first waveform represents the Electromagnetic Torque and rotor speed characteristics of the Squirrel cage Induction motor.

**Fig 17: Simulink model of Cascaded multilevel inverter fed induction motor**

Fig. 17 shows the simulink model of the Cascaded multilevel inverter fed to an induction motor.

**Fig 18: Line voltages of inverter**

**Fig 19: Three phase voltage of inverter**

Fig. 18 shows the line-line voltages of the CMLI and Fig. 19 shows the three phase voltages of the CMLI.

**Fig 20: Stator current**

**Fig 21: Speed of the motor**

Fig 20 shows the stator current characteristics of the induction motor and Fig 21 shows the speed curve of the induction motor. It is having the speed of 1450 r.p.m.
Fig 22 shows the electromagnetic torque characteristics of the induction motor.

V. CONCLUSION

A series connection of three-level inverters has been proposed for a medium-voltage SQIM drive with increased voltage capacity. The topology ensured high-power operations with medium-voltage output having several voltage levels. The reduction in the ratings of the dc bus capacitor and reduced imbalance problems in the dc bus are some of the advantages of the proposed topology over the existing topologies. The disadvantage of the proposed topology is that it requires additional output transformers which introduce additional cost and losses. However, these transformers do not have complex underutilized windings like that required in cascaded H-bridge topologies. In this paper conventional and the cascaded multilevel inverter topologies were discussed and results were placed. Finally a Matlab/Simulink model is developed and simulation results are presented.

REFERENCES


