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ELEVEN– LEVEL CASCADED H-BRIDGE INVERTER FED INDUCTION MOTOR USING PHASE SHIFT PWM TECHNIQUE

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ABSTRACT

Multilevel converters are increasingly being considered for high power applications because of their ability to operate at higher output voltages while producing lower levels of harmonic components in the switch output voltages. Many carriers based and sinusoidal PWM techniques for multilevel inverters have been developed very intensively in recent years. A phase shifted carrier PWM techniques is used for reducing the total harmonic distortion. A phase shifted carrier PWM technique for a eleven level Cascaded H-Bridge inverter fed induction motor drive is simulated using MATLAB/SIMULINK. FFT Spectrum for the outputs is analyzed to study for reduction in harmonics.

Keywords: Induction motor, Multilevel inverter, Multilevel SPWM, Phase shift technique, THD.

1. INTRODUCTION

Numerous industrial applications have begun to require higher power apparatus in recent years. Some medium voltage motor drives and utility applications require medium voltage and megawatt power level. For a medium voltage grid, it is troublesome to connect only one power semiconductor switch directly. As a result, a multilevel power converter structure has been introduced as an alternative in high power and medium voltage situations [1]. A voltage level of three is considered to be the smallest number in multilevel converter topologies.

A multilevel converter can switch either its input or output nodes between multiple (more than two) levels of voltage or current [2-4]. As the number of levels reaches infinity, the output THD approaches zero. The number of the achievable voltage levels, however, is limited by voltage-imbalance problems, voltage clamping requirements, circuit layout and packaging constraints complexity of the controller, and, of course, capital and maintenance costs. Three different major multilevel converter structures have been applied in industrial applications: cascaded H-bridges converter with separate dc sources, diode clamped, and flying capacitors. Nowadays, the industry requires power equipment increasingly high, in the megawatt range. The rapid evolution of semiconductor devices manufacturing technologies and the designer's orientation has enabled the development of new structures of converters with a great performance compared to conventional structures. So, these new technologies of semiconductor are more suited to high power applications and they enable the design of multilevel inverter.

The constraints due to commutation phenomena are also reduced and each component supports a much smaller fraction of the DC-bus voltage when the number of levels is higher. For this reason, the switches support more high reverse voltages in high-power applications and the converter output signals are with good spectral qualities. Thus, the using of this type of inverter, associated with a judicious control of power components, allows deleting some harmonics. In the last few years, the necessity of increasing the power quality enhancement in industry has sustained the continuous development of multilevel inverters due to high efficiency with low switching frequency control method. The multilevel inverters improve the AC power quality by performing the power conversion in small voltage steps resulted in lower harmonics. The output voltage on the

AC side can take several discrete levels of equal magnitude. The harmonic content of this output voltage waveform is greatly reduced, a smaller filter size and a lower EMI, if compared with a two level voltage waveform.

Several topologies for multi-level inverters have been proposed over the years the most popular being the diode clamped, flying capacitor and cascaded H-bridge structures. One aspect which sets the cascaded H-bridge apart from other multi-level inverters is the capability of utilizing different DC voltages on the individual H-bridge cells which results in splitting the power conversion amongst higher-voltage lower-frequency and lower-voltage higher frequency Inverters.

A multilevel inverter is a power electronic device built to synthesize a desired AC voltage from several levels of DC voltages. Such inverters have been the subject of research in the last several years where the DC levels were considered to be identical in that all of them were capacitors, batteries, solar cells, etc. In Recent Years, industry has begun to demand higher power equipment, which now reaches the megawatt level. Controlled ac drives in the megawatt range are usually connected to the medium-voltage network. Multilevel inverters include an array of power semiconductors and capacitor voltage sources, the output of which generate voltages with stepped waveforms. The commutation of the switches permits the addition of the capacitor voltages, which reach high voltage at the output, while the power semiconductors must withstand only reduced voltages

In this paper eleven level cascaded H-Bridge inverter fed induction motor load by using phase shifted PWM technique.

2. CASCADED H -BRIDGE INVERTER

Cascaded multilevel inverter, the full bridge configuration with a separate DC source, which may be batteries, fuel cells or solar cells and are connected in series. Each full bridge inverter (FBI) unit can generate a three level output: +Vdc, 0 or –Vdc by connecting the DC source to the AC load side by different combinations of the four switches S1, S2, S3 and S4.Using the top level as the example, turning on S1 and S4 yields +Vdc output. Turning on S2 and S3 yields -Vdc output. Turning off all switches yields 0 volts output. The AC output voltage at other levels can be obtained in the same manner. The number of voltage levels at the load generally defines the number of FBIs in cascade.

If N is the number of DC sources, the number of output voltage levels is m=2N+1. The number of FBI units N is (m-1)/2 where m is the sum of the number of positive, negative and zero levels in multilevel inverter output. Each H- bridge unit generates a quasi-square waveform by phase shifting its positive and negative phase legs" switching timings. Each switching device always conducts for 180° (or half cycle) regardless of the pulse width of the quasi-square wave. This switching method makes all of the switching devices current stress equal.

The number of converters N also depends on:

1) the injected voltage and current harmonic distortion requirements.

2) The magnitude of the injected voltage required.

3) The available power switch voltage ratings. The chosen inverter structure is simple since no real power needs to be supplied other than the losses.

The main features of cascaded multilevel inverters are:

1. Least number of components is required to achieve the same number of voltage levels.

2. Optimized circuit layout and packaging are possible

3. Soft-switching techniques can be used to reduce switching losses and device stresses.

4. The modular structure of the inverter leads to advantages in terms of manufacturing and flexibility of application.

The AC outputs of different full-bridge converters in the same phase are connected in series such that the synthesized voltage waveform is the sum of the individual converter outputs. Note that the number of output-

phase voltage levels is defined in a different way from those of the two previous converters (i.e. diode clamped and flying capacitor).

2. 1 Eleven Level Cascaded H- Bridge Inverter

The converter consists of five series connected H-Bridge cells which are fed by independent voltage sources. The outputs of the H-Bridge cells are connected in series such that the synthesized voltage waveform is the sum of all of the individual cell outputs V=Vdc1+Vdc2+Vdc3+Vdc4+Vdc5 where the output voltage of the first cell is labeled V_{dc1} and the output voltage of the second cell is denoted by $_{Vdc2.}$The output voltage of the third cell is denoted by V_{dc3} and the output voltage of the fourth cell is denoted by V_{dc4} and the output voltage of the fifth cell is denoted by V_{dc5}.There are eleven level of output voltage 5 V_{dc} ,4V_{dc}, 3V_{dc}, 2V_{dc}, V_{dc}, 0,-V_{dc},-2V_{dc},-3V_{dc},-4V_{dc} -5 V_{dc}. The resulting output ac voltage swings from- 5V_{dc} to +5V_{dc} with eleven levels and the staircase waveform is nearly sinusoidal, even without filtering.

The main advantages of using the cascade inverter include:

(1) No EMI problem or common-mode voltage/current problem exists.

(2) Low voltage switching devices can be used.

(3) No charge unbalance problem exists in both charge mode and drive mode.

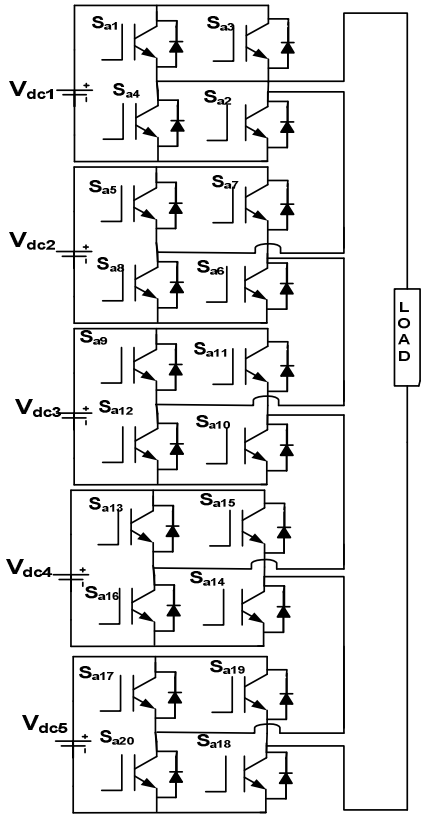

Fig 1: Single phase eleven level cascaded H-Bridge inverter

To produce a staircase output voltage considers one leg of the eleven-level inverter. The steps to synthesize the eleven-level voltages are as follows.

For an output voltage V_{ao}=0, turn on the switches S_2, S_4, S_6, S_8, S_{10}, S_{12}, S_{14}, S_{16}, S_{18}, $S_{20.}$

For an output voltage V_{ao}=V_{dc}, turn on the switches S_1, S_2, S_6, S_8, S_{10}, S_{12}, S_{14}, S_{16}, S_{18}, $S_{20.}$

For an output voltage $V_{ao}=2V_{dc}$, turn on the switches S_1, S_2, S_5, S_6, S_{10}, S_{12}, S_{14}, S_{16}, S_{18}, S_{20}.

For an output voltage $V_{ao}=3V_{dc}$, turn on the switches S_1, S_2, S_5, S_6, S_9, S_{10}, S_{14}, S_{16}, S_{18}, S_{20}.

For an output voltage $V_{ao}=4V_{dc}$, turn on the switches S_1, S_2, S_5, S_6, S_9, S_{10}, S_{13}, S_{14}, S_{18}, S_{20}.

For an output voltage $V_{ao}=5V_{dc}$, turn on the switches S_1, S_2, S_5, S_6, S_9, S_{10}, S_{13}, S_{14}, S_{17}, S_{18}.

For an output voltage $V_{ao}=-V_{dc}$, turn on the switches S_3, S_4, S_5, S_7, S_9, S_{11}, S_{13}, S_{15}, S_{17}, S_{19}.

For an output voltage $V_{ao}=-2V_{dc}$, turn on the switches S_3, S_4, S_7, S_8, S_9, S_{11}, S_{13}, S_{15}, S_{17}, S_{19}.

For an output voltage $V_{ao}=-3V_{dc}$, turn on the switches S_3, S_4, S_7, S_8, S_{11}, S_{12}, S_{13}, S_{15}, S_{17}, S_{19}.

For an output voltage $V_{ao}=-4V_{dc}$, turn on the switches S_3, S_4, S_7, S_8, S_{11}, S_{12}, S_{15}, S_{16}, S_{17}, S_{19}.

For an output voltage $V_{ao}=-5V_{dc}$, turn on the switches S_3, S_4, S_7, S_8, S_{11}, S_{12}, S_{15}, S_{16}, S_{19}, S_{20}.

Table 1: Switching states of Eleven- level Cascaded H-Bridge inverter

S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	S13	S14	S15	S16	S17	S18	S19	S20	Output voltage
0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
1	1	0	0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	V_{dc}
1	1	0	0	1	1	0	0	0	1	0	1	0	1	0	1	0	1	0	1	$2V_{dc}$
1	1	0	0	1	1	0	0	1	1	0	0	0	1	0	1	0	1	0	1	$3V_{dc}$
1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	0	1	0	1	$4V_{dc}$
1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	$5V_{dc}$
0	0	1	1	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	$-V_{dc}$
0	0	1	1	0	0	1	1	1	0	1	0	1	0	1	0	1	0	1	0	$-2V_{dc}$
0	0	1	1	0	0	1	1	0	0	1	1	1	0	1	0	1	0	1	0	$-3V_{dc}$
0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	1	0	1	0	$-4V_{dc}$
0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	$-5V_{dc}$

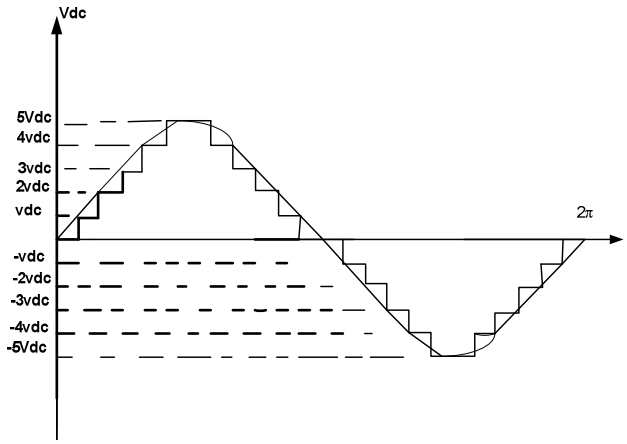

Fig 2: line-neutral voltage waveform of eleven- level CHB inverter

3. MULTI CARRIER PWM STRATEGY

Several multicarrier techniques have been developed to reduce the distortion in multilevel inverters, based on the classical SPWM with triangular carriers. Some methods use carrier disposition and others use phase shifting of multiple carrier signals. Multicarrier carrier pwm is widely used modulation strategy for multilevel inverter. In this several triangular carrier signals are compared with one sinusoidal modulating signal. The number of carriers required to produce n-level output is n-1.All carriers have the same amplitude Ac and same frequency fc. Whenever the reference signal is greater than the carrier signal the pulse is generated.

3.1 Phase Shifted Carrier PWM (PSCPWM)

In general a multi level inverter with n voltage levels requires (n-1) triangular carriers. In this method all the triangular carriers have the same frequency and same amplitude but they are in phase shift by any two adjacent carrier waves given by $\emptyset_{cr} = \frac{360^0}{(n-1)}$ .The gate signals are generated by comparing the modulating wave with the carrier waves. For an eleven-level inverter, ten triangular carriers are needed with a 36° phase displacement between any two adjacent carriers. In this case the phase displacement of V_{cr1} = 0°, V_{cr2} = 36°, V_{cr3} = 72° V_{cr4} = 108°, V_{cr5} =144°, V_{cr6} = 180°, V_{cr7} = 216°, V_{cr8} = 252°, $V_{cr8=}$288°, $V_{cr9=}$324°, $V_{cr9=}$360°.

4. TOTAL HARMONIC DISTORTION

The total harmonic distortion, or THD, of a signal is a measurement of the harmonic distortion present and is defined as the ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency. The main criterion for assessing the quality of the voltage delivered by an inverter is the total harmonic distortion (THD).The low order harmonics amplitude will decrease when the number of levels increase. The performance of multilevel inverter can be improved by cancelling or reducing low order harmonics.

The THD is a ratio between the Root Mean Square (RMS) of the harmonics and the fundamental signal. For An inverter that has a fundamental output voltage V1 and harmonics V2, V3,. . . , we define the THD as follows:

$$THD = \frac{\sqrt{\sum_{K=2}^{N} V_K^2}}{V_1} \qquad (1)$$

4. SIMULATION RESULTS

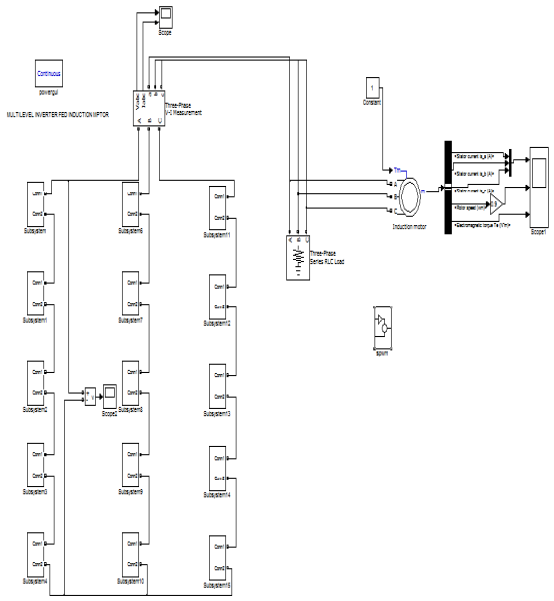

Fig 3: Simulink of Eleven- level cascaded H-Bridge inverter with induction motor

As above Fig.3 shows the 3 Simulink of Eleven- level cascaded H-Bridge inverter with induction motor

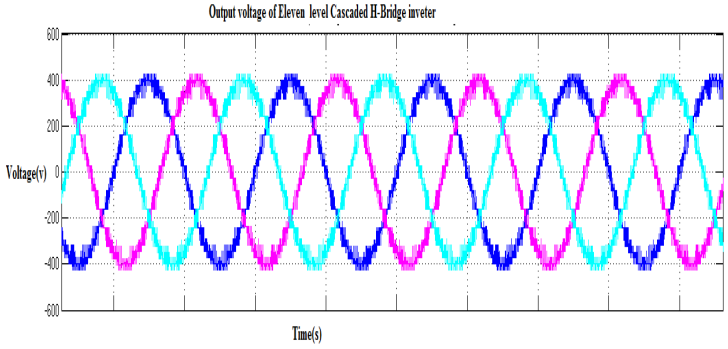

Fig 4: Output current of Eleven- level cascaded H-Bridge inverter

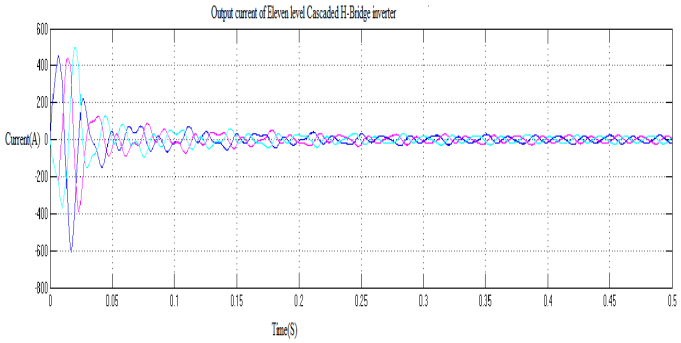

Fig 5: Output voltage of Eleven- level cascaded H-Bridge inverter

As above Fig.4 and 5 shows the Output voltage and current of Eleven- level cascaded H-Bridge inverter.

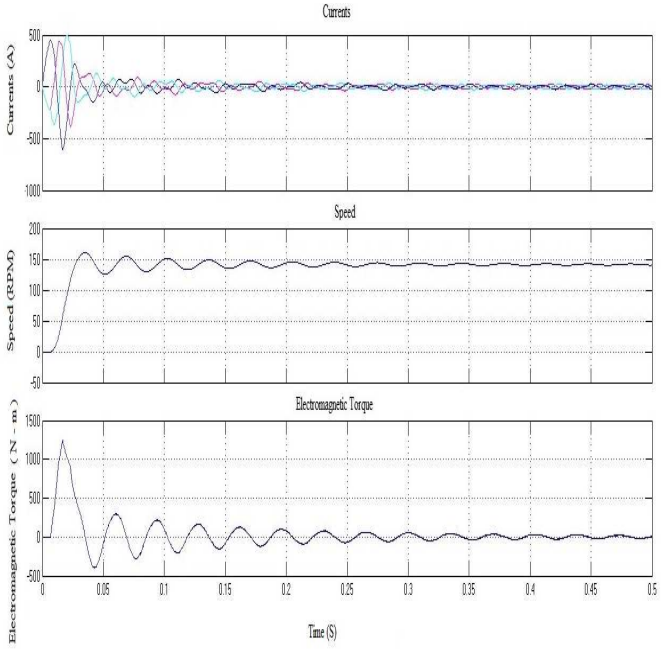

Fig 6: Currents and electromagnetic torque and speed for Eleven- level cascaded H-Bridge inverter with induction motor

The above Fig. 6 shows the armature currents of induction motor, electromagnetic torque and speed for Eleven-level cascaded H-Bridge inverter with induction motor drive.

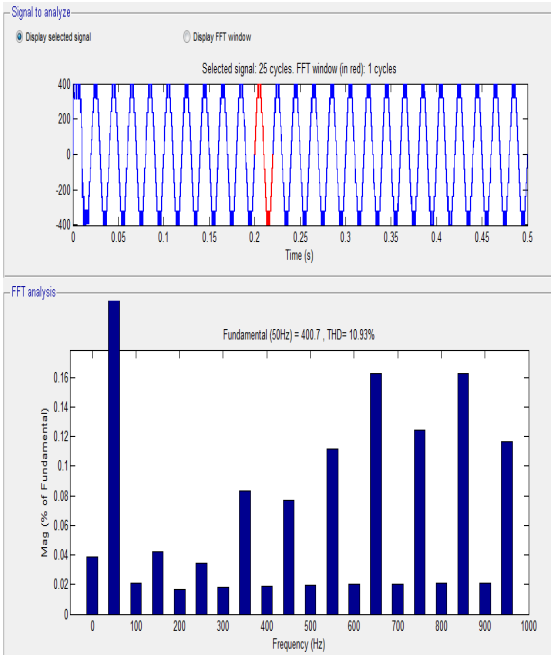

Fig 7: FFT analysis of Eleven-level inverter with induction motor drive

As above Fig 6 shows that FFT analysis of Eleven-level inverter with induction motor drive The THD of this multilevel inverter is 10.93%.

6. CONCLUSION

This paper has provided a brief summary of Cascaded H- Bridge inverter fed induction motor drive. Phase shifted carrier PWM technique for a Eleven level CHB inverter fed induction motor drive is simulated and the results are presented. The FFT spectrums for the outputs are analyzed. The simulation results shows that THD of Eleven- level CHB is 10.93%.Eleven -level Cascaded H-bridge Multilevel inverter gives the less value of THD. This CHB inverter has many merits such as reduce number of switches, lower EMI, less harmonic distortion. These latter can be easily eliminated with a simple low pass filter.

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